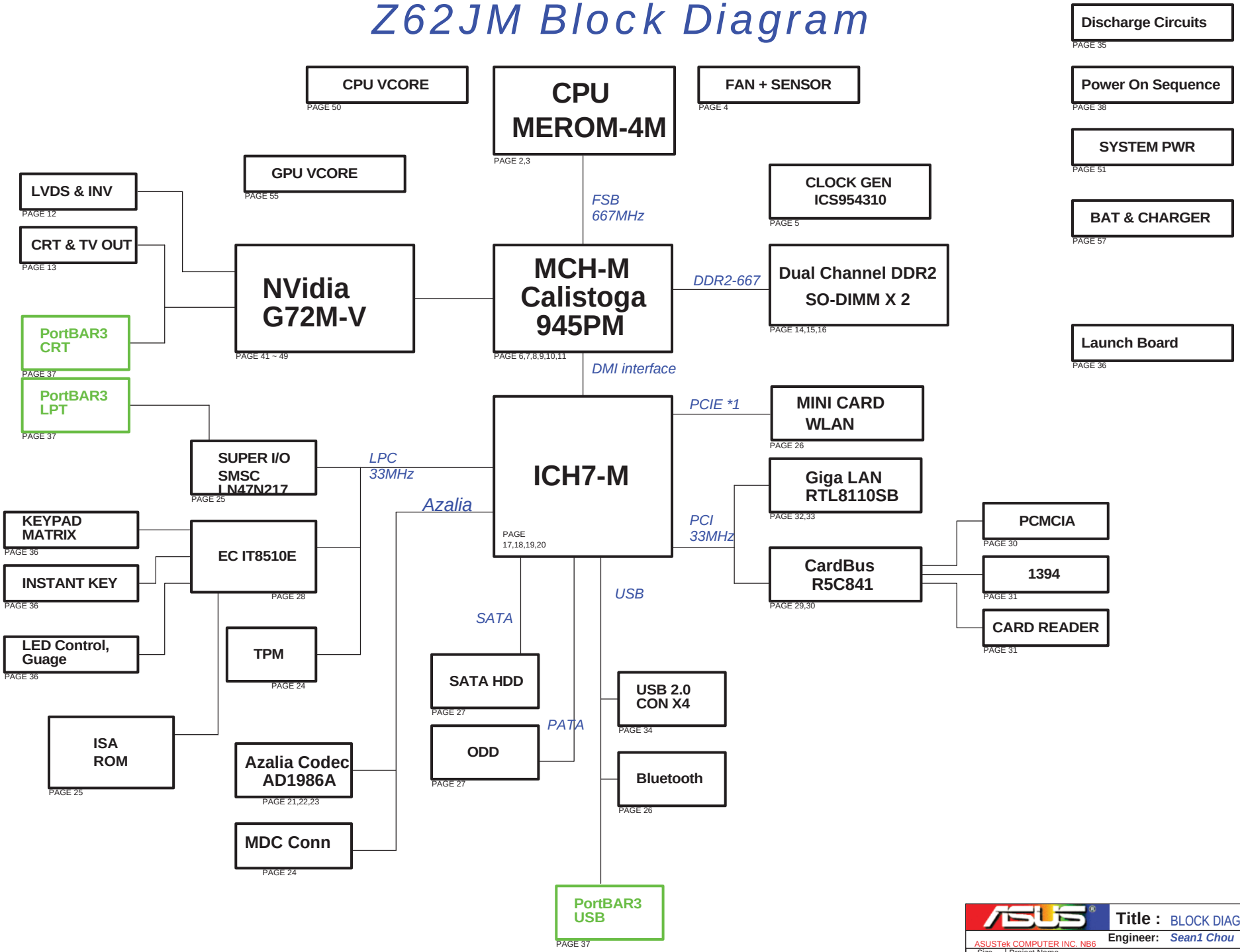
Z62JM Block Diagram



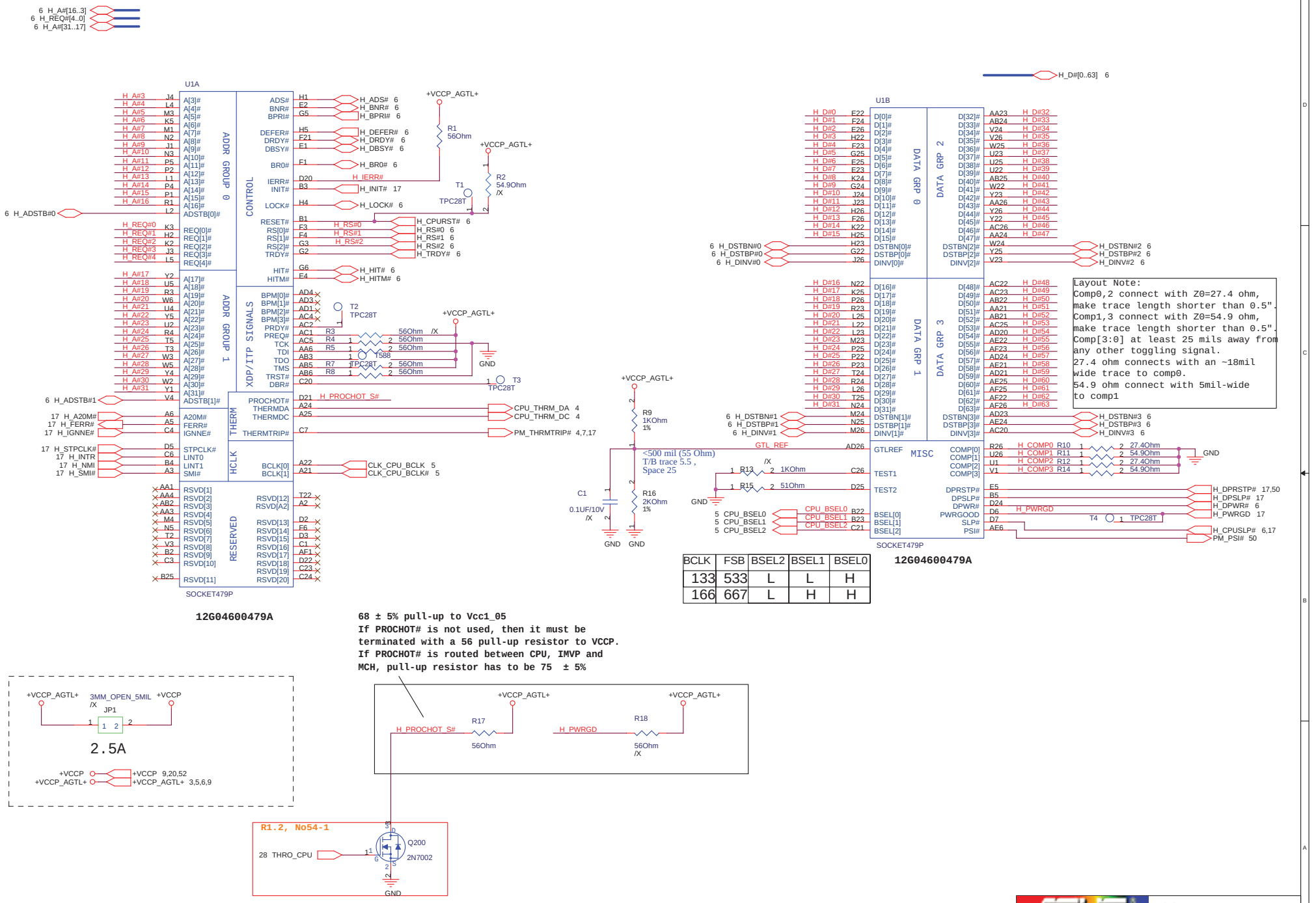
ASUSTek COMPUTER INC. NB6

Title : BLOCK DIAGRAM

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 1 of 69



YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

+VCCP_AGTL+ +VCCP_AGTL+ 2,5,6,9

+VCORE +VCORE 50

+1.5VS +1.5VS 7,9,20,26,35,52,56

R1.1,No43

unmount CE1,CE4

R2.1, No94-1

unmount CE54

C2~C31 22uF --> 10uF

Vcc Core Decoupling Caps
Place these on bottom side.

Place these caps on North side Secondary

CE1 470UF/2.5V /X

Place these caps on North side Secondary

C2 C3 C4 C5 C6 C7 C8 C9 10UF/6.3V

Place these caps on North side Primary

C12 C13 C14 C15 C16 10UF/6.3V

Place these caps on South side Primary

C18 C19 C20 C21 C22 10UF/6.3V

Place these caps on South side Secondary

C24 C25 C26 C27 C28 C29 C30 C31 10UF/6.3V

Place these caps on South side Secondary

CE4 470UF/2.5V /X

checklist suggests
0.1uF X5R

checklist suggests
10uF POSCAP

U1C

SOCKET479P

12G04600479A

U1D

SOCKET479P

12G04600479A

+VCCP_AGTL+ V6 G21 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

+VCCA_CPU B26

RN1A 0Ohm

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]

H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6

RN2D RN2C RN2B RN2A RN1D RN1C RN1B 0Ohm

VR_VID0 50 VR_VID1 50 VR_VID2 50 VR_VID3 50 VR_VID4 50 VR_VID5 50 VR_VID6 50

VCCSENSE AF7 R19 100Ohm +VCORE

VSSSENSE AF7

VCCSENSE 50 VSSSENSE 50

R20 100Ohm GND

VCCSENCE/VSSSENCE
need to be routed as
27.4ohm

Layout note:Route VCCSENSE and VSSSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.

Place pull-up/down resisters within 1 inch of CPU.

+1.5VS JP2 +VCCA_CPU

SHORT_PIN

0.12A

Close to B26 (VCCA)

+VCCA_CPU 120mA / 20mil

+VCCA_PROC

C41 10UF/10V C40 0.01UF/16V GND

+VCCP_AGTL+

CE54 470UF/2.5V /X GND

C34 C35 C36 C37 C38 C39 0.1UF/10V GND

+V1.05S (VCCP_CPU)
Decoupling Capacitor
(Place near CPU)

Title : Yonah CPU (2)

ASUSTek COMPUTER INC. NB6 Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

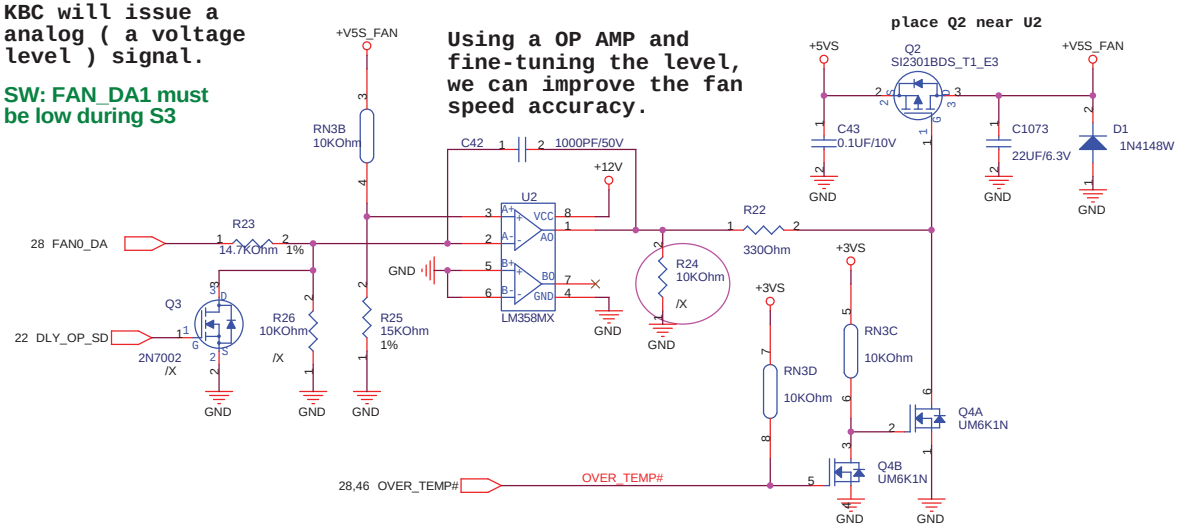
Date: Wednesday, August 16, 2006 Sheet 3 of 69

Fan Speed Control

KBC will issue a analog (a voltage level) signal.

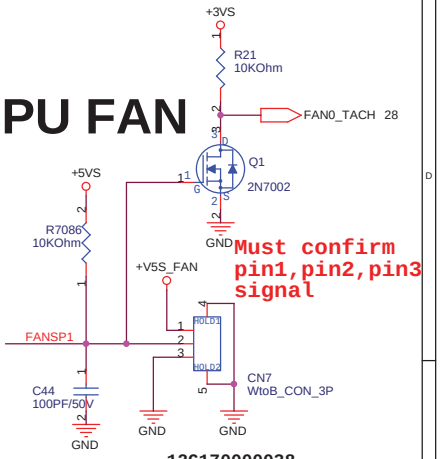
SW: FAN_DA1 must be low during S3

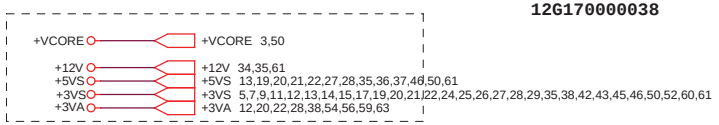
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.



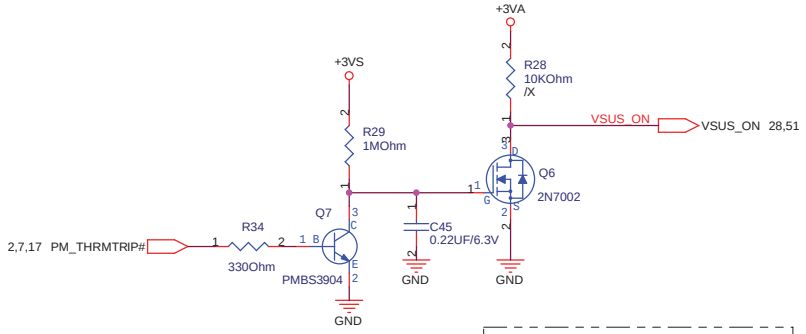
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

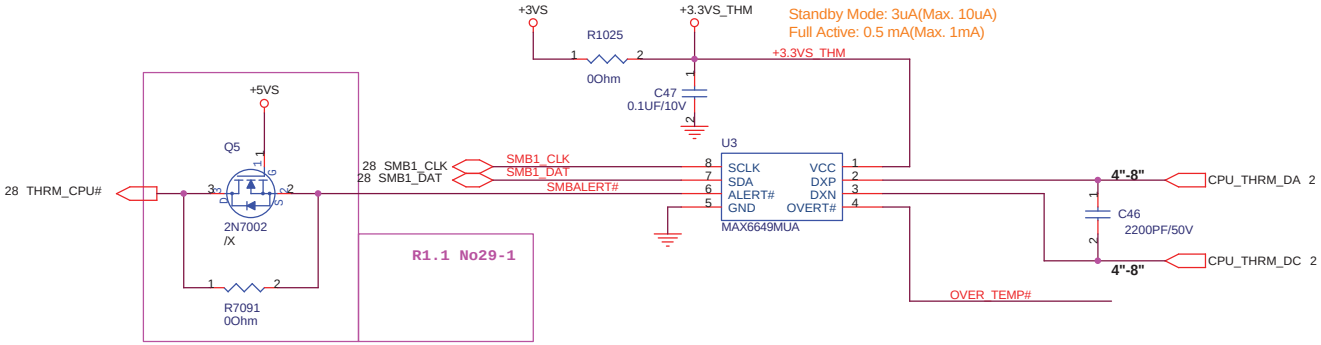
CPU FAN





U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSTek COMPUTER INC. NB6	Title : THER-SENSOR,FAN	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 4 of 69	

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD1(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	None

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

PLACE termination close to source IC

Pin34 is PWRSAVE#

27MHz selected by SELPCIE0_LCD# and SELLCD_27#

IC1 — ICS954310CGLFT

R72 change to 39Ohm R1.1 No30-1

R77,R79,R83 change to 470hm.

R81 change to 27Ohm

R1.2, No59

clock gen version change to ICS954310CGLFT

PEREQ Register:
00100000 PCIE*3 is controlled <= check:PCIE*3 is controlled by CLKREQ#
00000010 PCIE*4 is controlled <= reserved only

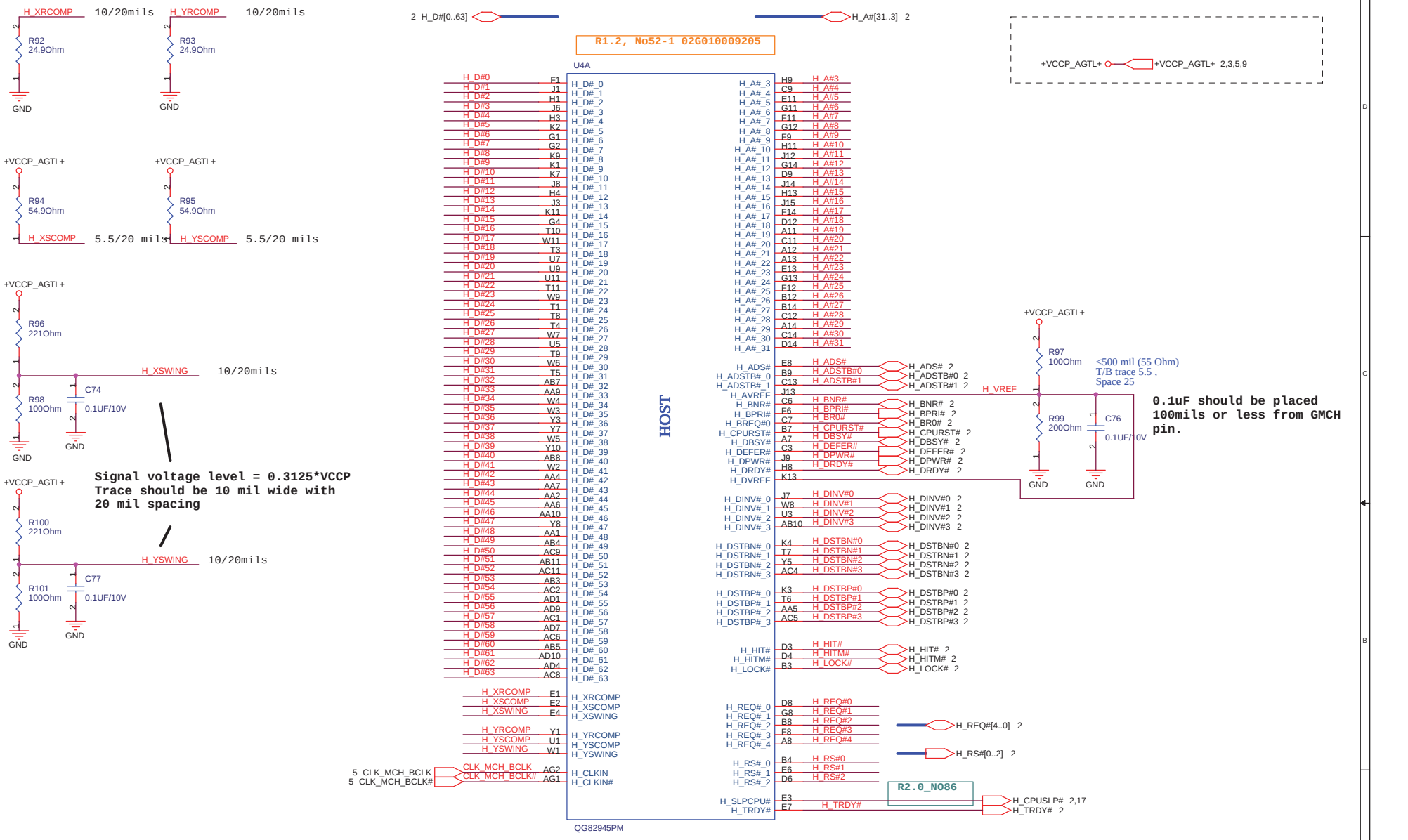
No2.1, No97

ASUSTek COMPUTER INC. NB6 — Engineer: Sean1 Chou

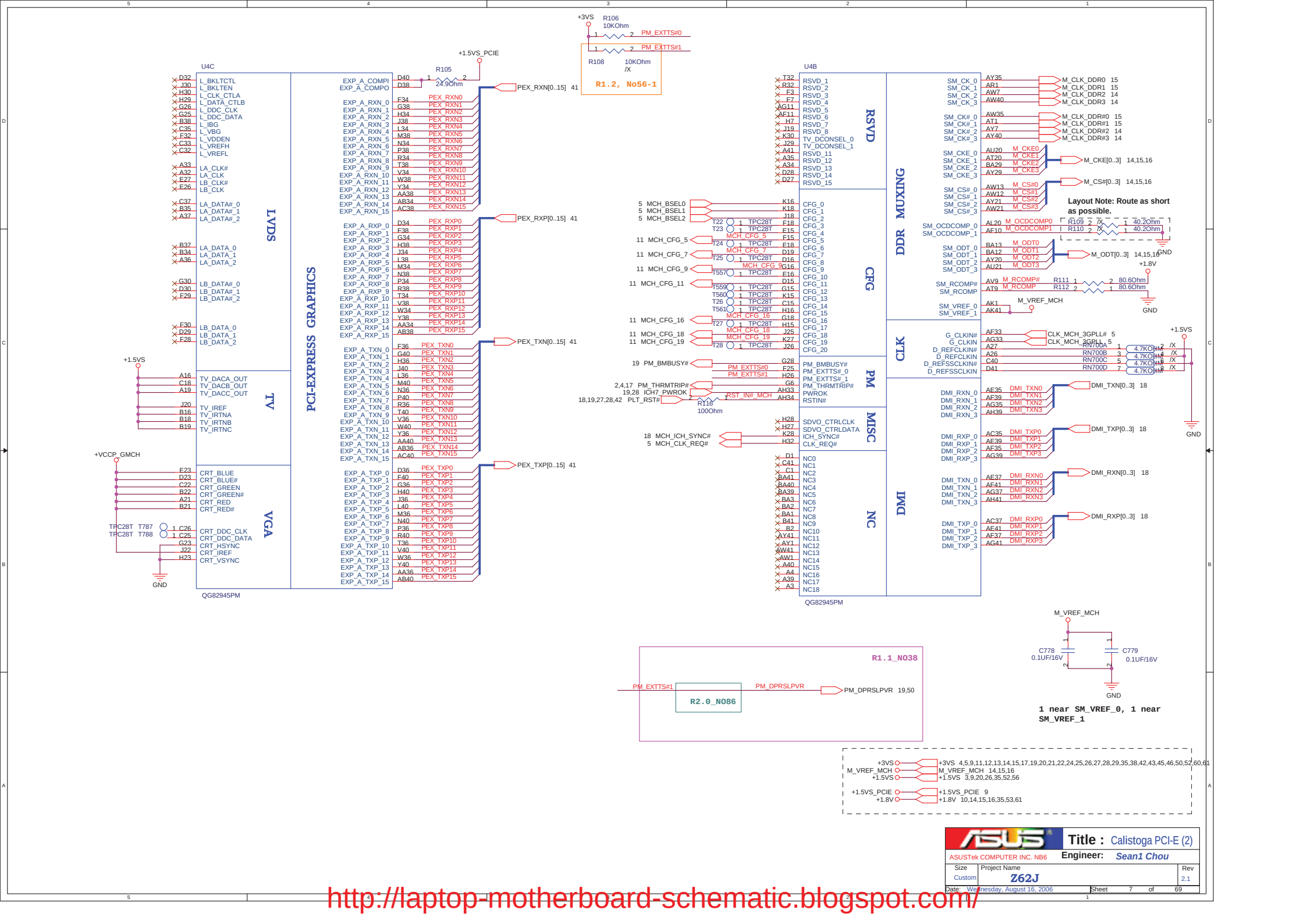
Title : CLOCK GEN

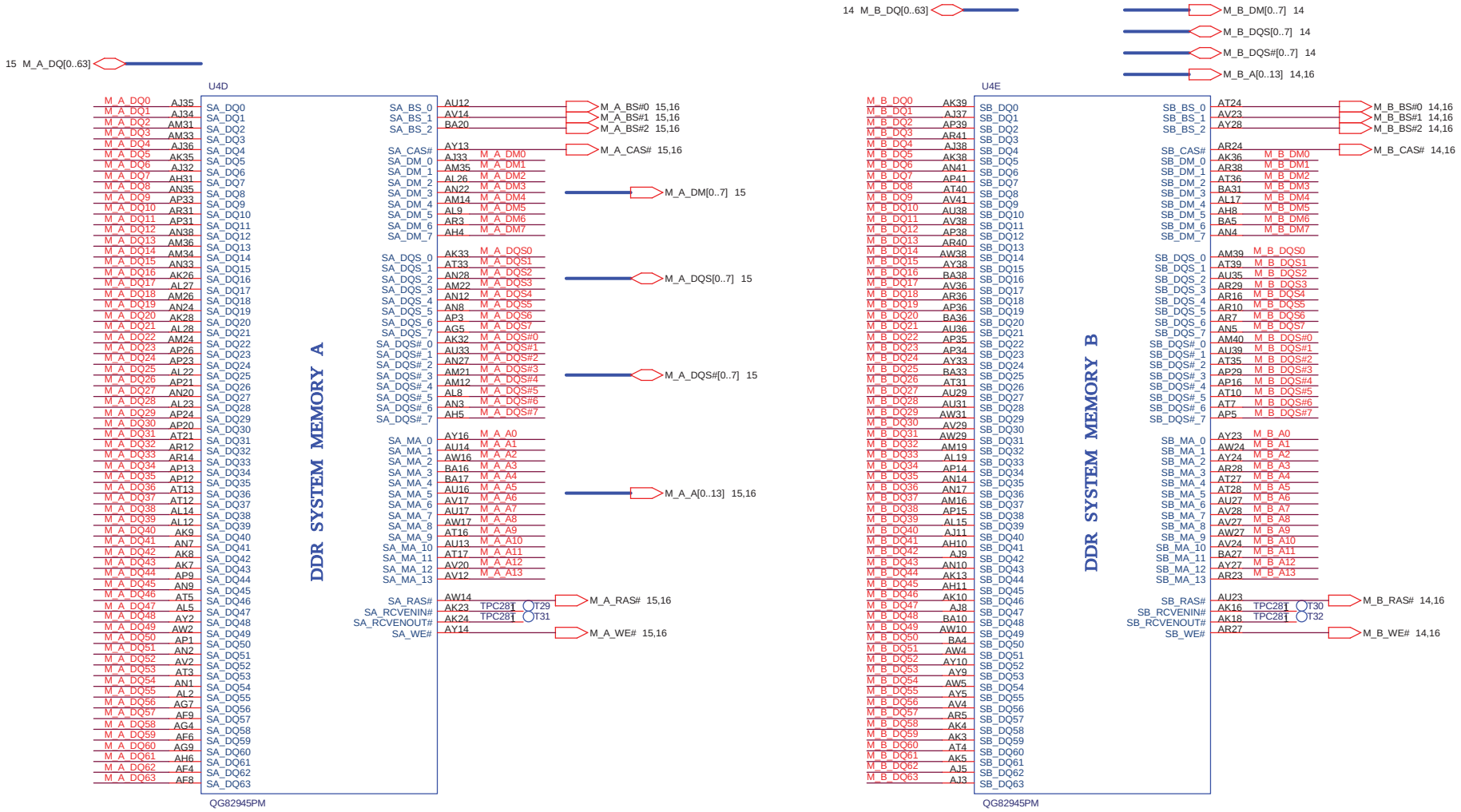
Size: Custom | Project Name: Z62J | Rev: 2.1

Date: Wednesday, August 16, 2006 | Sheet 5 of 69



Title :	Calistoga MCH (1)		
ASUSTek COMPUTER INC. NB6	Engineer:	Sean1 Chou	
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 6 of 69		





ASUSTek COMPUTER INC. NB6	Title : Calistoga DDR2 (3)	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 8 of 69	

VCCA_3GBG

NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

+VCCP — 3MM_OPEN_5MIL /X — JP28 — +VCCP_GMCH

Z62J use 1.05V

R2.1, No94 unmount CE8

+VCCP_AGTL+ 2,3,5,6 — +VCCP_GMCH 7,10 — +1.5VS_PCIE 7 — +3VS 4,5,7,11,12,13,14,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52 — +2.5VS 35,44,46,54 — +1.5VS 3,7,20,26,35,52,56

+2.5VS — C956 4.7UF/10V — C901 0.1UF/10V — GND GND

VCCA_3GBG 2 mA

D77 — R1026 10Ohm — +VCCP_GMCH — BAT54C

+1.5VS — L88 120Ohm/100Mhz — +1.5VS_PCIE — VCC3G — 1500 mA

C955 0.1UF/10V — C904 10UF/10V — C905 10UF/10V — GND GND GND

+1.5VS_3GPLL — L90 30Ohm/100Mhz — VCCA3GPLL

C82 0.1UF/10V — C83 10UF/10V — GND GND

+1.5VS_VCCAUX — L91 100Ohm/100Mhz — VCCAUX

Place filter components close to GMCH

CE50 470UF/2.5V — C912 0.1UF/10V — GND GND

+1.5VS_DPLLA — L3 30Ohm/100Mhz — VCCA_DPLLA 50 mA

CE10 470UF/2.5V /X — C916 0.1UF/10V — GND GND

+1.5VS_DPLLB — L4 30Ohm/100Mhz — VCCA_DPLLB 50 mA

CE13 470UF/2.5V /X — C919 0.1UF/10V — GND GND

+1.5VS_HPLL — L5 120Ohm/100Mhz — VCCA_HPLL 45 mA

C920 22UF/6.3V — C85 0.1UF/10V — GND GND

+1.5VS_MPLL — L6 120Ohm/100Mhz — VCCA_MPLL 45 mA

C921 22UF/6.3V — C87 0.1UF/10V — GND GND

+1.5VS — VCCD_TVDAC — 24 mA

C84 0.022UF/25V — C909 0.1UF/10V — GND GND

+1.5VS — VCCDQ_TVDAC

C86 0.022UF/25V — C913 0.1UF/10V — GND GND

U4H

+1.5VS_PCIE	H22	VCCSYNC	
	C30	VCC_TXLVDS0	
GND	B30	VCC_TXLVDS1	
	A30	VCC_TXLVDS2	
	AJ41	VCC3G0	
	AB41	VCC3G1	
	Y41	VCC3G2	
	V41	VCC3G3	
	R41	VCC3G4	
	N41	VCC3G5	
	L41	VCC3G6	
+2.5VS	AC33	VCCA_3GPLL	
+1.5VS_3GPLL	G41	VCCA_3GBG	
	H41	VSSA_3GBG	
+VCCP_GMCH	F21	VCCA_CRTDAC0	
GND	F21	VCCA_CRTDAC1	
	G21	VSSA_CRTDAC	
GND +1.5VS_DPLLA	B26	VCCA_DPLLA	
+1.5VS_DPLLB	C39	VCCA_DPLLB	
+1.5VS_HPLL	AF1	VCCA_HPLL	
GND	A38	VCCA_LVDS	
	B39	VSSA_LVDS	
+1.5VS_MPLL	AF2	VCCA_MPLL	
+1.5VS	H20	VCCA_TVBG	
	G20	VSSA_TVBG	
+1.5VS	F19	VCCA_TVDACA0	
	F19	VCCA_TVDACA1	
	C20	VCCA_TVDACB0	
	D20	VCCA_TVDACB1	
	E20	VCCA_TVDACC0	
	F20	VCCA_TVDACC1	
+1.5VS	AH1	VCCD_HMPLL0	
	AH2	VCCD_HMPLL1	
	A28	VCCD_LVDS0	
	B28	VCCD_LVDS1	
GND	C28	VCCD_LVDS2	
+1.5VS	D21	VCCD_TVDAC	
+3VS	A23	VCC_HV0	
	B23	VCC_HV1	
	B25	VCC_HV2	
+1.5VS	H19	VCCD_QTVDAC	
+1.5VS_VCCAUX	AK31	VCCAUX0	
	AF31	VCCAUX1	
	AE31	VCCAUX2	
	AC31	VCCAUX3	
	AL30	VCCAUX4	
	AK30	VCCAUX5	
	AJ30	VCCAUX6	
	AH30	VCCAUX7	
	AG30	VCCAUX8	
	AF30	VCCAUX9	
	AE30	VCCAUX10	
	AD30	VCCAUX11	
	AC30	VCCAUX12	
	AG29	VCCAUX13	
	AF29	VCCAUX14	
	AE29	VCCAUX15	
	AD29	VCCAUX16	
	AC29	VCCAUX17	
	AG28	VCCAUX18	
	AF28	VCCAUX19	
	AE28	VCCAUX20	
	AH22	VCCAUX21	
	AJ21	VCCAUX22	
	AH21	VCCAUX23	
	AJ20	VCCAUX24	
	AH20	VCCAUX25	
	AH19	VCCAUX26	
	P19	VCCAUX27	
	P16	VCCAUX28	
	AH15	VCCAUX29	
	P15	VCCAUX30	
	AH14	VCCAUX31	
	AG14	VCCAUX32	
	AF14	VCCAUX33	
	AE14	VCCAUX34	
	Y14	VCCAUX35	
	AF13	VCCAUX36	
	AE13	VCCAUX37	
	AF12	VCCAUX38	
	AE12	VCCAUX39	
	AD12	VCCAUX40	

QG82945PM

POWER

+VCCP_AGTL+	AC14	VTT_0	
	AB14	VTT_1	
	W14	VTT_2	
	V14	VTT_3	
	T14	VTT_4	
	R14	VTT_5	
	P14	VTT_6	
	N14	VTT_7	
	M14	VTT_8	
	L14	VTT_9	
	AD13	VTT_10	
	AC13	VTT_11	
	AB13	VTT_12	
	AA13	VTT_13	
	Y13	VTT_14	
	W13	VTT_15	
	V13	VTT_16	
	U13	VTT_17	
	T13	VTT_18	
	R13	VTT_19	
	N13	VTT_20	
	M13	VTT_21	
	L13	VTT_22	
	AB12	VTT_23	
	AA12	VTT_24	
	Y12	VTT_25	
	W12	VTT_26	
	V12	VTT_27	
	U12	VTT_28	
	T12	VTT_29	
	R12	VTT_30	
	P12	VTT_31	
	N12	VTT_32	
	M12	VTT_33	
	L12	VTT_34	
	R11	VTT_35	
	P11	VTT_36	
	N11	VTT_37	
	M11	VTT_38	
	R10	VTT_39	
	P10	VTT_40	
	N10	VTT_41	
	M10	VTT_42	
	P9	VTT_43	
	N9	VTT_44	
	M9	VTT_45	
	R8	VTT_46	
	P8	VTT_47	
	N8	VTT_48	
	M8	VTT_49	
	P7	VTT_50	
	N7	VTT_51	
	M7	VTT_52	
	R6	VTT_53	
	P6	VTT_54	
	M6	VTT_55	
	A6	VTT_56	
	R5	VTT_57	
	P5	VTT_58	
	N5	VTT_59	
	M5	VTT_60	
	P4	VTT_61	
	N4	VTT_62	
	M4	VTT_63	
	R3	VTT_64	
	P3	VTT_65	
	N3	VTT_66	
	M3	VTT_67	
	R2	VTT_68	
	P2	VTT_69	
	M2	VTT_70	
	D2	VTT_71	
	AB1	VTT_72	
	R1	VTT_73	
	P1	VTT_74	
	N1	VTT_75	
	M1	VTT_76	

VTTLF_CAP3 — C88 0.47UF/16V — GND

VTTLF_CAP2 — C89 0.47UF/16V — GND

VTTLF_CAP1 — C90 0.22UF/6.3V — GND

PLACE IN CAVITY

C79 4.7UF/10V — C80 2.2UF/6.3V — GND

PLACE ON THE EDGE

800 mA +VCCP_AGTL+

C81 0.22UF/6.3V — CE8 330UF/2V — GND

post- R2.1: No 101 mount 150uF

Z62JM ER NO4 mount 330uF

+3VS — VCCHV 40 mA

C93 10UF/10V — C94 0.1UF/10V — GND GND

+3VS — R1027 10Ohm — D78 — +1.5VS — BAT54C

LVDS disabled

	SDVO disabled	SDVO enabled
VCCD_LVDS	GND	1.5V
VCCA_LVDS	GND	GND
VCCTX_LVDS	GND	GND

TV-OUT disabled

VCCD_TVDAC	1.5V
VCCD_QTVDAC	1.5V
VCCA_TVDACA,VCCA_TVDACB, VCCA_TVDACC	1.5V
VCCA_TVBG	1.5V
TV_IREF	1.5V
TCDACAOUT,TCDACBOUT, TCDACCOUT, TV_IRTNA,TV_IRTNB,TV_IRTNC	1.5V
VSSA_TVBG	GND

CRT disabled

VCCA_CRTDAC	VCCP_GMCH
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC,YSHYC	GND
RED,RED#,GREEN,GREEN#, BLUE,BLUE#	VCCP_GMCH

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

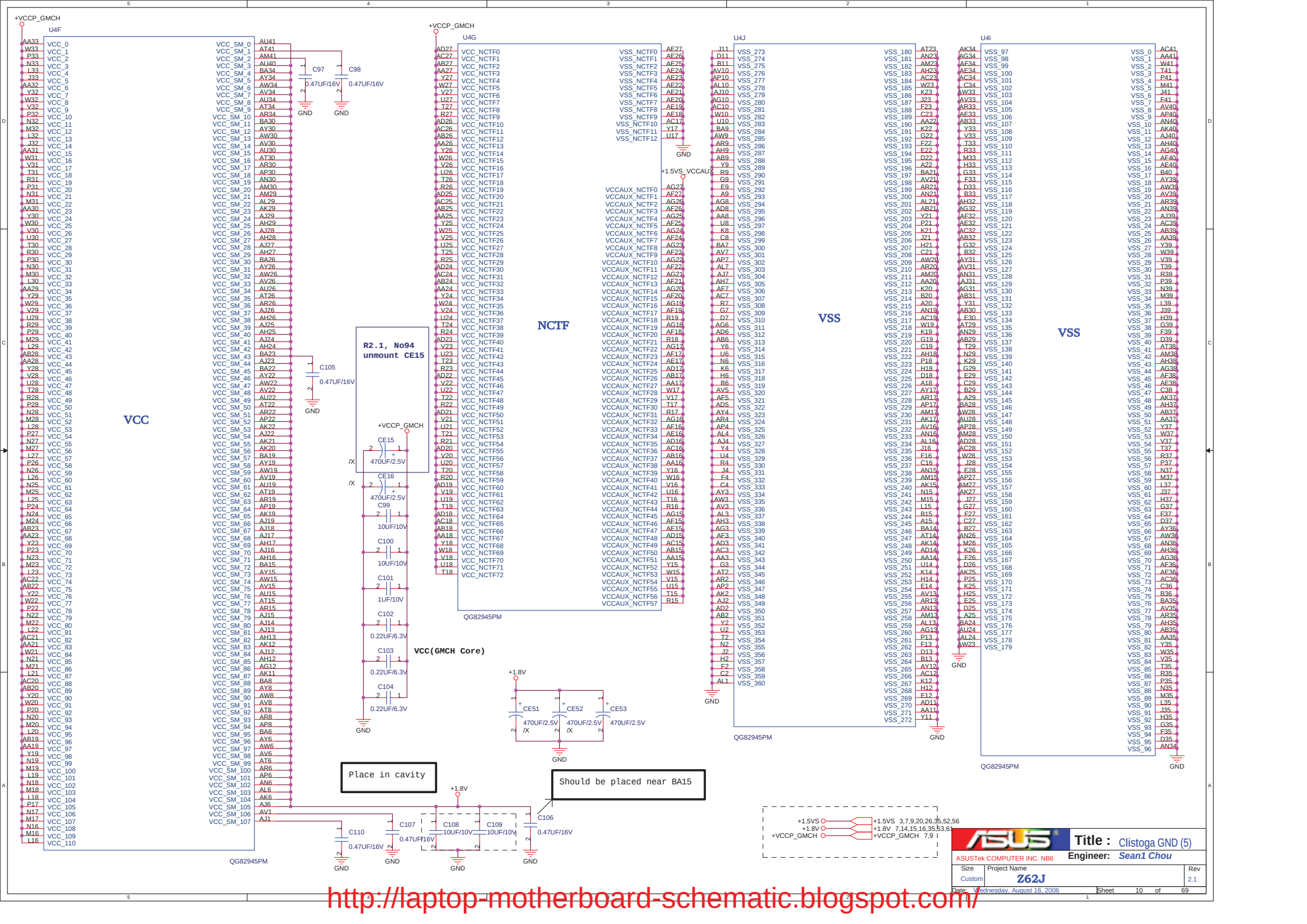
ASUSTek COMPUTER INC. NB6

Title : Calistoga Power (4)

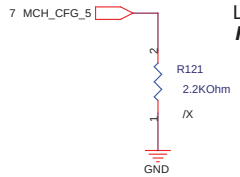
Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 9 of 69

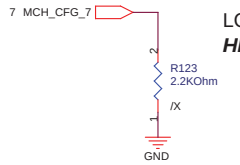


CFG5 : DMI X2 Select



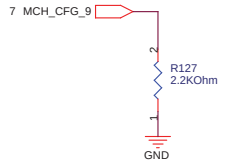
LOW = DMI X 2
HIGH = DMI X 4 (Default)

CFG7 : CPU STRAP



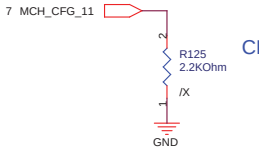
LOW = Reserved
HIGH = Mobility CPU (Default)

CFG9 : PCIE GRAPHIC LANE

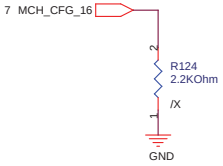


LOW = REVERSE LANES (Z62J default)
HIGH = NORMAL OPERATION

CFG11 : Reserved but need to be pull low

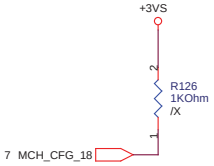


CFG16 : FSB DYNAMIC ODT



LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

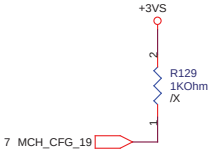
CFG18 : GMCH Core Voltage Level



LOW = 1.05V (Z62J default)
HIGH = 1.5V

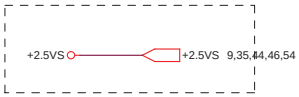
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG19 : DMI LANE REVERSAL



LOW = NORMAL
HIGH = LANES REVERSED

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



ASUSTek COMPUTER INC. NB6 | Engineer: *Sean1 Chou*

Title : Calistoga Strapping

Size	Project Name	Rev
Custom	Z62J	2.1

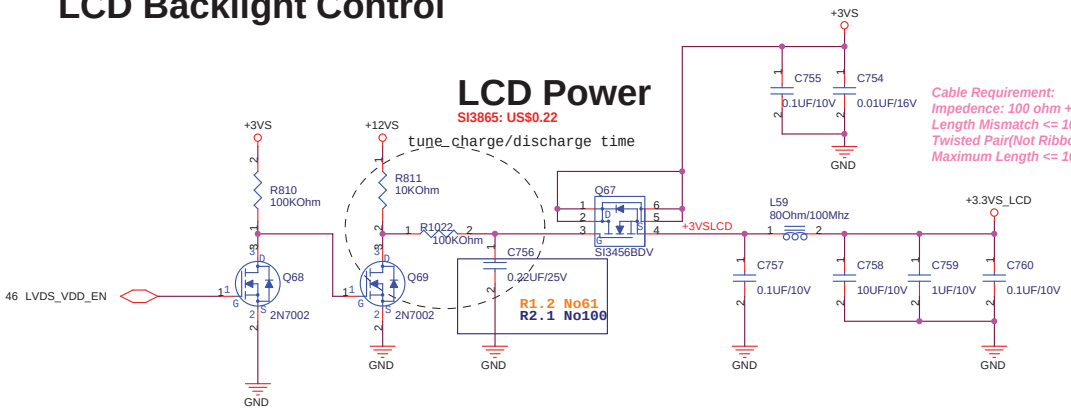
Date: Wednesday, August 16, 2006 | Sheet 11 of 69

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

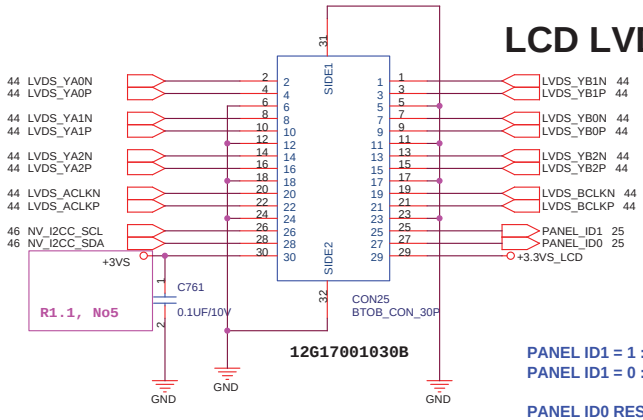
LCD Power

SI3865: US$0.22

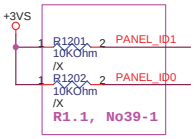


Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface



12G17001030B



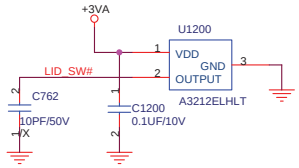
PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

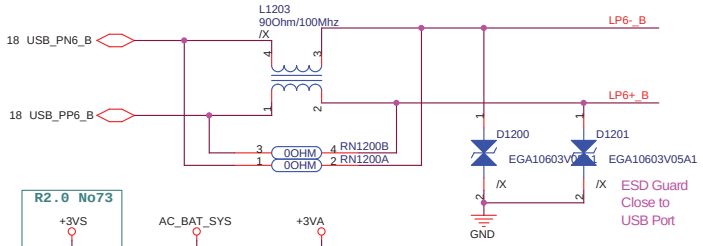
PANEL ID0 RESERVE FOR VENDOR

INVERTER Interface

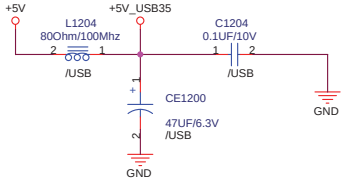
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

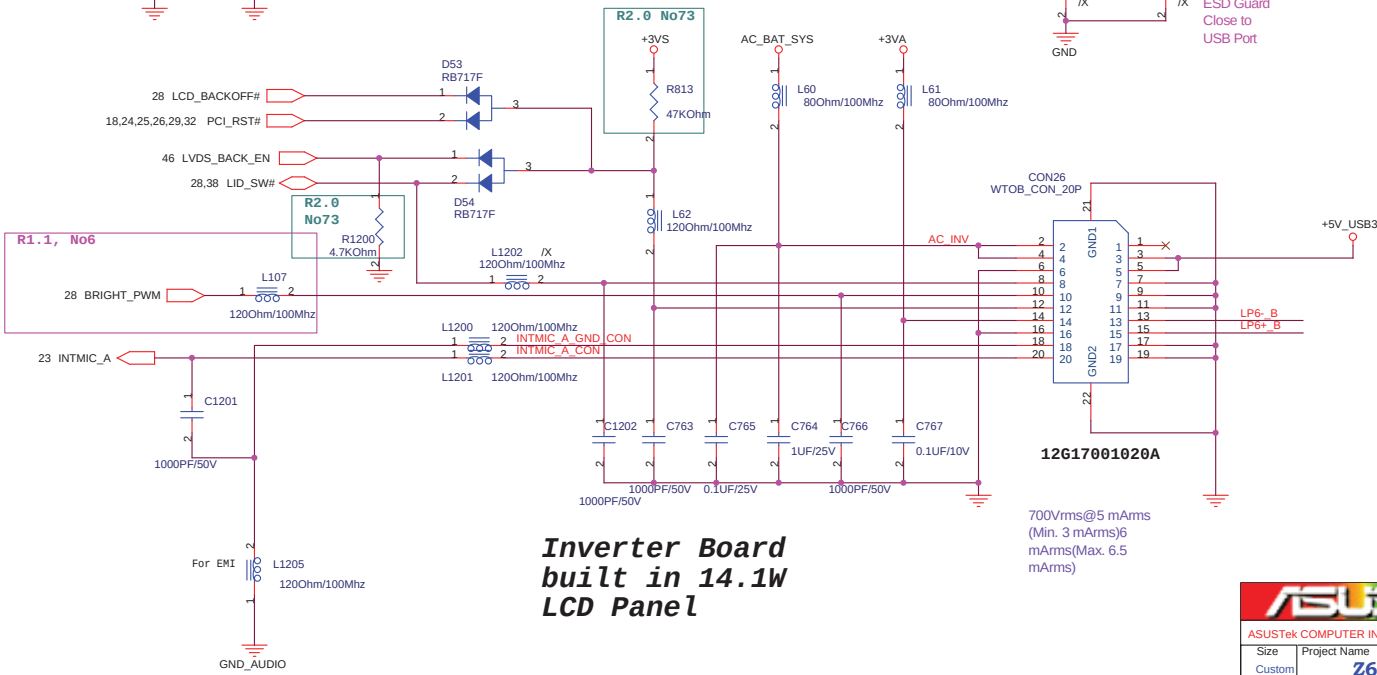
Magnatic Switch
For LID_SW# On/OFF





ESD Guard Close to USB Port





12G17001020A

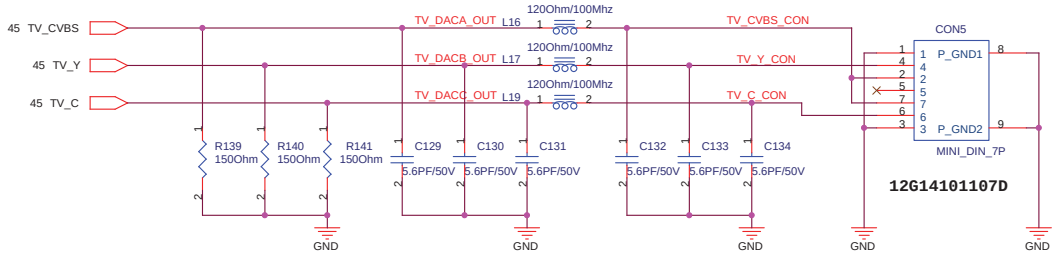
700Vrms@5 mArms
(Min. 3 mArms)6
mArms(Max. 6.5
mArms)

Inverter Board built in 14.1W LCD Panel

ASUSTek COMPUTER INC. NB6	Title : LVDS & INVERTER	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 12 of 69	

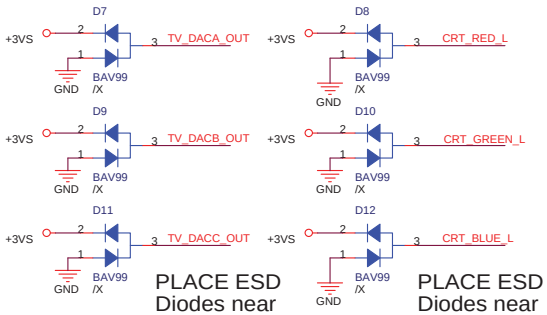
TV OUT

checklist suggests
150ohm/100MHz & 6pF



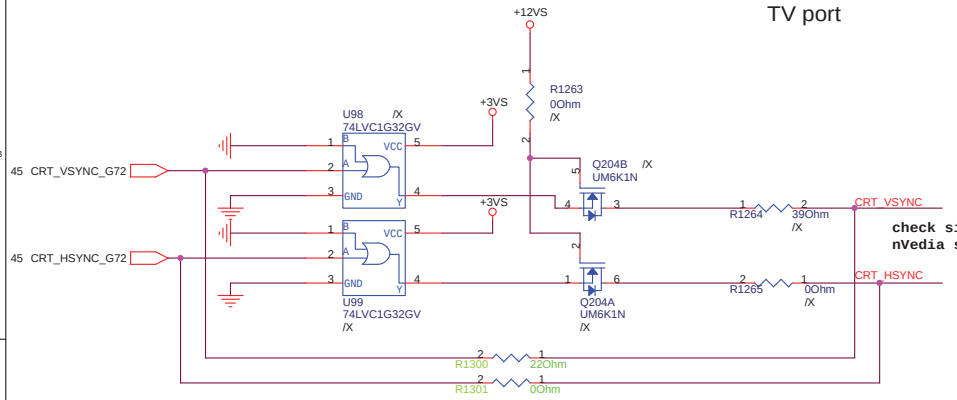
12G14101107D

Place Terminator
close to
Connector

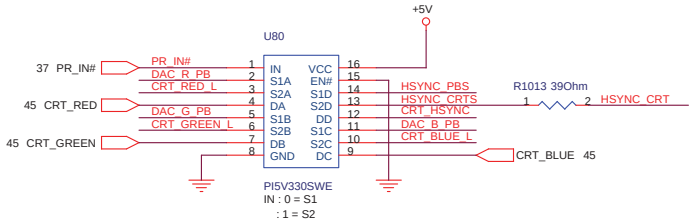


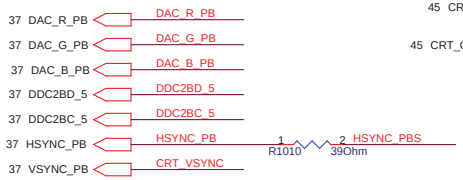
PLACE ESD
Diodes near
TV port

PLACE ESD
Diodes near
VGA port



check signal integrity,
nVedia suggest 33ohm

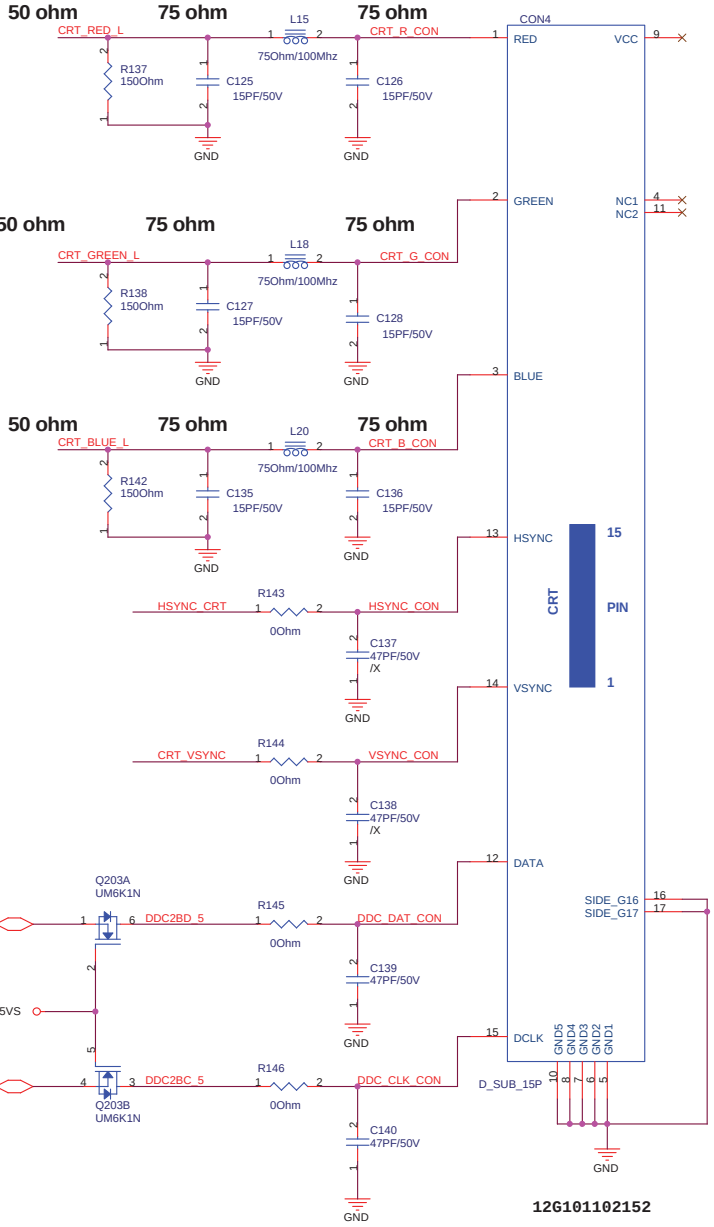




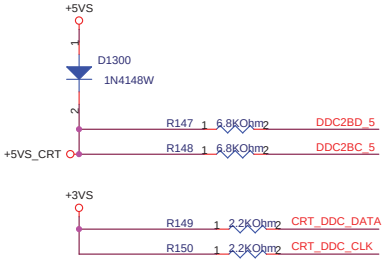
To PortBar III

CRT OUT

checklist suggests 47ohm/100MHz



12G101102152



ASUSTek COMPUTER INC. NB6

Title : CRT & TV OUT

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 13 of 69

NO STUFF *

M_CLK_DDR3

PLACE NEAR SO-DIMM_0

M_CLK_DDR#3

M_CLK_DDR2

PLACE NEAR SO-DIMM_0

M_CLK_DDR#2

8,16 M_B_A[0..13]

M_VREF_DIMM1 — M_VREF_DIMM1 7,15,16
+1.8V — +1.8V 7,10,15,16,35,53,61
+3VS — +3VS 4,5,7,9,11,12,13,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

M_B_DQ[0..63] 8

U5A

M_B_A0	102	A0	DQ0	5	M_B_DQ58
M_B_A1	101	A1	DQ1	7	M_B_DQ63
M_B_A2	100	A2	DQ2	17	M_B_DQ56
M_B_A3	99	A3	DQ3	19	M_B_DQ60
M_B_A4	98	A4	DQ4	4	M_B_DQ62
M_B_A5	97	A5	DQ5	6	M_B_DQ61
M_B_A6	94	A6	DQ6	14	M_B_DQ57
M_B_A7	92	A7	DQ7	16	M_B_DQ59
M_B_A8	93	A8	DQ8	23	M_B_DQ50
M_B_A9	91	A9	DQ9	25	M_B_DQ55
M_B_A10	105	A10/AP	DQ10	35	M_B_DQ49
M_B_A11	90	A11	DQ11	37	M_B_DQ53
M_B_A12	89	A12	DQ12	20	M_B_DQ51
M_B_A13	116	A13	DQ13	22	M_B_DQ54
	86	A14	DQ14	36	M_B_DQ52
	84	A15	DQ15	38	M_B_DQ48
8,16 M_B_BS#2	85	A16_BA2	DQ16	43	M_B_DQ43
			DQ17	45	M_B_DQ41
8,16 M_B_BS#0	107	BA0	DQ18	55	M_B_DQ40
8,16 M_B_BS#1	106	BA1	DQ19	57	M_B_DQ46
7,16 M_CS#2	110	S0#	DQ20	44	M_B_DQ42
7,16 M_CS#3	115	S1#	DQ21	46	M_B_DQ47
7 M_CLK_DDR2	30	CK0	DQ22	56	M_B_DQ45
7 M_CLK_DDR#2	32	CK0#	DQ23	58	M_B_DQ44
7 M_CLK_DDR3	164	CK1	DQ24	61	M_B_DQ34
7 M_CLK_DDR#3	166	CK1#	DQ25	63	M_B_DQ38
7,16 M_CKE2	79	CKE0	DQ26	73	M_B_DQ32
7,16 M_CKE3	80	CKE1	DQ27	75	M_B_DQ36
8,16 M_B_CAS#	113	CAS#	DQ28	62	M_B_DQ35
8,16 M_B_RAS#	108	RAS#	DQ29	64	M_B_DQ39
8,16 M_B_WE#	109	WE#	DQ30	74	M_B_DQ37
+3VS	198	SA0	DQ31	76	M_B_DQ33
	200	SA1	DQ32	123	M_B_DQ27
5,15,19,24,26 SMB_CLK_S	197	SCL	DQ33	125	M_B_DQ30
5,15,19,24,26 SMB_DAT_S	195	SDA	DQ34	135	M_B_DQ28
			DQ35	137	M_B_DQ29
7,16 M_ODT2	114	ODT0	DQ36	124	M_B_DQ31
7,16 M_ODT3	119	ODT1	DQ37	126	M_B_DQ26
			DQ38	134	M_B_DQ25
M_B_DM7	10	DM0	DQ39	136	M_B_DQ24
M_B_DM6	26	DM1	DQ40	141	M_B_DQ18
M_B_DM5	52	DM2	DQ41	143	M_B_DQ19
M_B_DM4	67	DM3	DQ42	151	M_B_DQ20
M_B_DM3	130	DM4	DQ43	153	M_B_DQ16
M_B_DM2	147	DM5	DQ44	140	M_B_DQ22
M_B_DM1	170	DM6	DQ45	142	M_B_DQ23
M_B_DM0	185	DM7	DQ46	152	M_B_DQ21
			DQ47	154	M_B_DQ17
M_B_DQS7	13	DQS0	DQ48	157	M_B_DQ9
M_B_DQS6	31	DQS1	DQ49	159	M_B_DQ15
M_B_DQS5	51	DQS2	DQ50	173	M_B_DQ10
M_B_DQS4	70	DQS3	DQ51	175	M_B_DQ8
M_B_DQS3	131	DQS4	DQ52	158	M_B_DQ14
M_B_DQS2	148	DQS5	DQ53	160	M_B_DQ11
M_B_DQS1	169	DQS6	DQ54	174	M_B_DQ13
M_B_DQS0	188	DQS7	DQ55	176	M_B_DQ12
M_B_DQS#7	11	DQS#0	DQ56	179	M_B_DQ6
M_B_DQS#6	29	DQS#1	DQ57	181	M_B_DQ7
M_B_DQS#5	49	DQS#2	DQ58	189	M_B_DQ4
M_B_DQS#4	68	DQS#3	DQ59	191	M_B_DQ1
M_B_DQS#3	129	DQS#4	DQ60	180	M_B_DQ2
M_B_DQS#2	146	DQS#5	DQ61	182	M_B_DQ3
M_B_DQS#1	167	DQS#6	DQ62	192	M_B_DQ5
M_B_DQS#0	186	DQS#7	DQ63	194	M_B_DQ0

Group7 Group6 Group5 Group4 Group3 Group2 Group1 Group0

DDR_DIMM_200P_A

R1.1 No17

For Data Swap

12G025122007

8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]

Layout Note: Place these High-Freq decoupling Caps near the GMCH

U5B

	VDD1	VSS16	18
	VDD2	VSS17	24
	VDD3	VSS18	41
	VDD4	VSS19	53
	VDD5	VSS20	42
	VDD6	VSS21	54
	VDD7	VSS22	59
	VDD8	VSS23	65
	VDD9	VSS24	60
	VDD10	VSS25	66
	VDD11	VSS26	127
	VDD12	VSS27	139
		VSS28	128
	VDDSPD	VSS29	145
		VSS30	165
	NC1	VSS31	171
	NC2	VSS32	172
	NC3	VSS33	177
	NC4	VSS34	187
	NCTEST	VSS35	178
		VSS36	190
	VREF	VSS37	9
		VSS38	21
	GND0	VSS39	33
	GND1	VSS40	155
		VSS41	34
	NP_NC1	VSS42	132
	NP_NC2	VSS43	144
		VSS44	156
	VSS1	VSS45	168
	VSS2	VSS46	2
	VSS3	VSS47	3
	VSS4	VSS48	15
	VSS5	VSS49	27
	VSS6	VSS50	39
	VSS7	VSS51	149
	VSS8	VSS52	161
	VSS9	VSS53	28
	VSS10	VSS54	40
	VSS11	VSS55	138
	VSS12	VSS56	150
	VSS13	VSS57	162
	VSS14		
	VSS15		

DDR_DIMM_200P_A

12G025122007

+1.8V
+3VS
C143 2.2UF/6.3V
C144 0.1UF/10V
C145 2.2UF/6.3V
C146 0.1UF/10V
VREF -> 10/10 mils
M_VREF_DIMM1
GND

Layout Note: Place these Caps near SO DIMM 1

Layout Note: Place these resistors near the GMCH

+1.8V
C151 0.1UF/10V
C152 0.1UF/10V
C153 0.1UF/10V
C154 0.1UF/10V
GND

Layout Note: Place these Caps near SO DIMM 1

+1.8V
C149 0.1UF/10V
C150 0.1UF/10V
C147 0.1UF/10V
C148 0.1UF/10V
GND

+1.8V
C155 2.2UF/6.3V
C156 2.2UF/6.3V
C157 2.2UF/6.3V
C158 2.2UF/6.3V
C159 2.2UF/6.3V
GND

ASUSTek COMPUTER INC. NB6

Title : DDR2_SO-DIMM(1)

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 14 of 69

8,16 M_A_A[0..13]

8 M_A_DM[0..7]

8 M_A_DQS[0..7]

8 M_A_DQS#[0..7]

M_A_DQ[0..63] 8

+1.8V +1.8V 7,10,14,16,35,53,61

+3VS +3VS 4,5,7,9,11,12,13,14,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

M_VREF_DIMM0 M_VREF_DIMM0 7,14,16

NO STUFF *

M_CLK_DDR0

PLACE NEAR SO-DIMM_1

M_CLK_DDR#0

M_CLK_DDR1

PLACE NEAR SO-DIMM_1

M_CLK_DDR#1

U8A

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
86 A14
84 A15
85 A16_BA2

8,16 M_A_BS#2

8,16 M_A_BS#0 107 BA0
8,16 M_A_BS#1 106 BA1
7,16 M_CS#0 110 S0#
7,16 M_CS#1 115 S1#
7 M_CLK_DDR1 30 CK0
7 M_CLK_DDR#1 32 CK0#
7 M_CLK_DDR0 164 CK1
7 M_CLK_DDR#0 166 CK1#
7,16 M_CKE0 79 CKE0
7,16 M_CKE1 80 CKE1
8,16 M_A_CAS# 113 CAS#
8,16 M_A_RAS# 108 RAS#
8,16 M_A_WE# 109 WE#
198 SA0
200 SA1
5,14,19,24,26 SMB_CLK_S 197 SCL
5,14,19,24,26 SMB_DAT_S 195 SDA

7,16 M_ODT0 114 ODT0
7,16 M_ODT1 119 ODT1

R1.1 No17

M_A_DM7 10 DM0
M_A_DM6 26 DM1
M_A_DM5 52 DM2
M_A_DM4 67 DM3
M_A_DM3 130 DM4
M_A_DM2 147 DM5
M_A_DM1 170 DM6
M_A_DM0 185 DM7

M_A_DQS7 13 DQS0
M_A_DQS6 31 DQS1
M_A_DQS5 51 DQS2
M_A_DQS4 70 DQS3
M_A_DQS3 131 DQS4
M_A_DQS2 148 DQS5
M_A_DQS1 169 DQS6
M_A_DQS0 188 DQS7
M_A_DQS#7 11 DQS#0
M_A_DQS#6 29 DQS#1
M_A_DQS#5 49 DQS#2
M_A_DQS#4 68 DQS#3
M_A_DQS#3 129 DQS#4
M_A_DQS#2 146 DQS#5
M_A_DQS#1 167 DQS#6
M_A_DQS#0 186 DQS#7

5 DQ0
7 DQ1
17 DQ2
19 DQ3
4 DQ4
6 DQ5
14 DQ6
16 DQ7
23 DQ8
25 DQ9
35 DQ10
37 DQ11
20 DQ12
22 DQ13
36 DQ14
38 DQ15
43 DQ16
45 DQ17
55 DQ18
57 DQ19
44 DQ20
46 DQ21
56 DQ22
58 DQ23
61 DQ24
63 DQ25
73 DQ26
75 DQ27
62 DQ28
64 DQ29
74 DQ30
76 DQ31
123 DQ32
125 DQ33
135 DQ34
137 DQ35
124 DQ36
126 DQ37
134 DQ38
136 DQ39
141 DQ40
143 DQ41
151 DQ42
153 DQ43
140 DQ44
142 DQ45
152 DQ46
154 DQ47
157 DQ48
159 DQ49
173 DQ50
175 DQ51
158 DQ52
160 DQ53
174 DQ54
176 DQ55
179 DQ56
181 DQ57
189 DQ58
191 DQ59
180 DQ60
182 DQ61
192 DQ62
194 DQ63

M_A_DQ63 Group7
M_A_DQ59
M_A_DQ57
M_A_DQ60
M_A_DQ58
M_A_DQ62
M_A_DQ61
M_A_DQ56

M_A_DQ55 Group6
M_A_DQ51
M_A_DQ52
M_A_DQ53
M_A_DQ54
M_A_DQ50
M_A_DQ49
M_A_DQ48

M_A_DQ43 Group5
M_A_DQ41
M_A_DQ42
M_A_DQ40
M_A_DQ46
M_A_DQ47
M_A_DQ44
M_A_DQ45

M_A_DQ32 Group4
M_A_DQ35
M_A_DQ36
M_A_DQ37
M_A_DQ39
M_A_DQ38
M_A_DQ33
M_A_DQ34

M_A_DQ31 Group3
M_A_DQ26
M_A_DQ24
M_A_DQ25
M_A_DQ27
M_A_DQ30
M_A_DQ29
M_A_DQ28

M_A_DQ22 Group2
M_A_DQ19
M_A_DQ21
M_A_DQ20
M_A_DQ18
M_A_DQ23
M_A_DQ16
M_A_DQ17

M_A_DQ11 Group1
M_A_DQ9
M_A_DQ14
M_A_DQ8
M_A_DQ10
M_A_DQ15
M_A_DQ12
M_A_DQ13

M_A_DQ2 Group0
M_A_DQ3
M_A_DQ5
M_A_DQ1
M_A_DQ7
M_A_DQ6
M_A_DQ4
M_A_DQ0

DDR_DIMM_200P

GND GND

For Data Swap

12G025C22000

GMCH=====>SODIMM1=>SODIMM0

+1.8V

U8B

112 VDD1
111 VDD2
117 VDD3
96 VDD4
95 VDD5
118 VDD6
81 VDD7
82 VDD8
87 VDD9
103 VDD10
88 VDD11
104 VDD12
199 VDDSPD
83 NC1
120 NC2
50 NC3
69 NC4
163 NCTEST
1 VREF
201 GND0
202 GND1
203 NP_NC1
204 NP_NC2
47 VSS1
133 VSS2
183 VSS3
77 VSS4
12 VSS5
48 VSS6
184 VSS7
78 VSS8
71 VSS9
72 VSS10
121 VSS11
122 VSS12
196 VSS13
193 VSS14
8 VSS15

18 VSS16
24 VSS17
41 VSS18
53 VSS19
42 VSS20
54 VSS21
59 VSS22
65 VSS23
60 VSS24
66 VSS25
127 VSS26
139 VSS27
128 VSS28
145 VSS29
165 VSS30
171 VSS31
172 VSS32
177 VSS33
187 VSS34
178 VSS35
190 VSS36
9 VSS37
21 VSS38
33 VSS39
155 VSS40
34 VSS41
132 VSS42
144 VSS43
156 VSS44
168 VSS45
2 VSS46
3 VSS47
15 VSS48
27 VSS49
39 VSS50
149 VSS51
161 VSS52
28 VSS53
40 VSS54
138 VSS55
150 VSS56
162 VSS57

DDR_DIMM_200P

+3VS

C209 2.2UF/6.3V
C210 0.1UF/10V

VREF -> 10/10 mils
M_VREF_DIMM0

C211 2.2UF/6.3V
C212 0.1UF/10V

GND GND GND GND GND

12G025C22000

Layout Note: Place these Caps near SO DIMM 0

+1.8V

C213 0.1UF/10V
C214 0.1UF/10V
C215 0.1UF/10V
C216 0.1UF/10V

GND GND GND GND

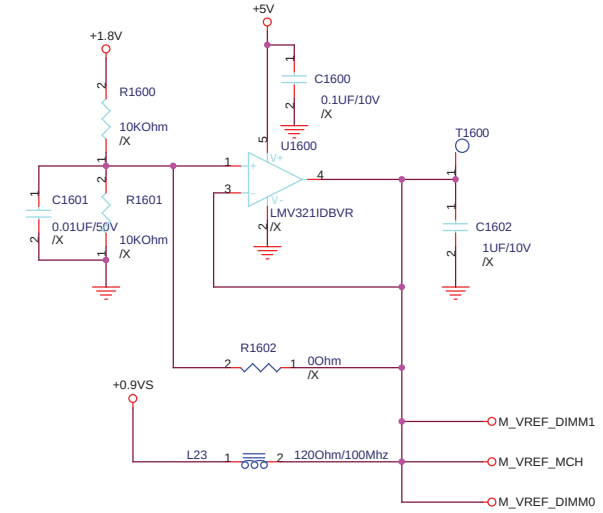
Layout Note: Place these Caps near SO DIMM 0

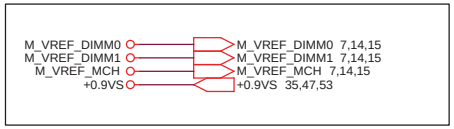
+1.8V

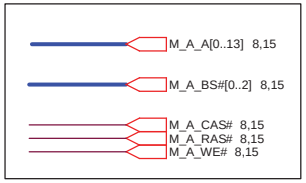
C217 2.2UF/6.3V
C218 2.2UF/6.3V
C219 2.2UF/6.3V
C220 2.2UF/6.3V
C221 2.2UF/6.3V

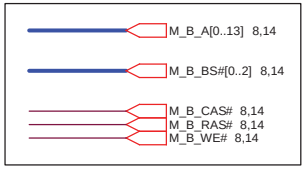
GND GND GND GND GND

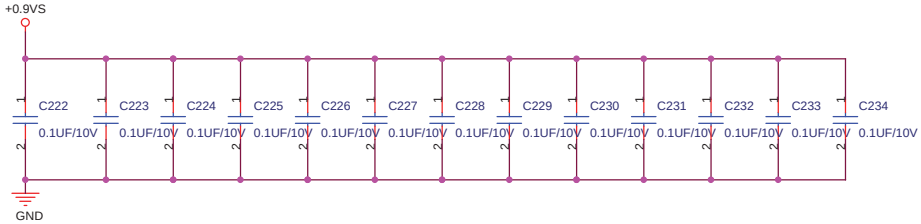
ASUSTek COMPUTER INC. NB6	Title : DDR2 SO-DIMM(0)	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 15 of 69	



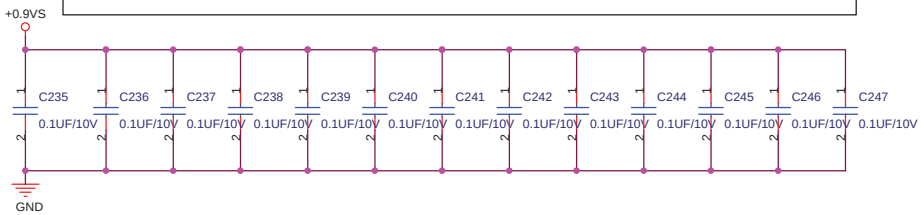


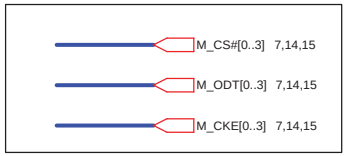


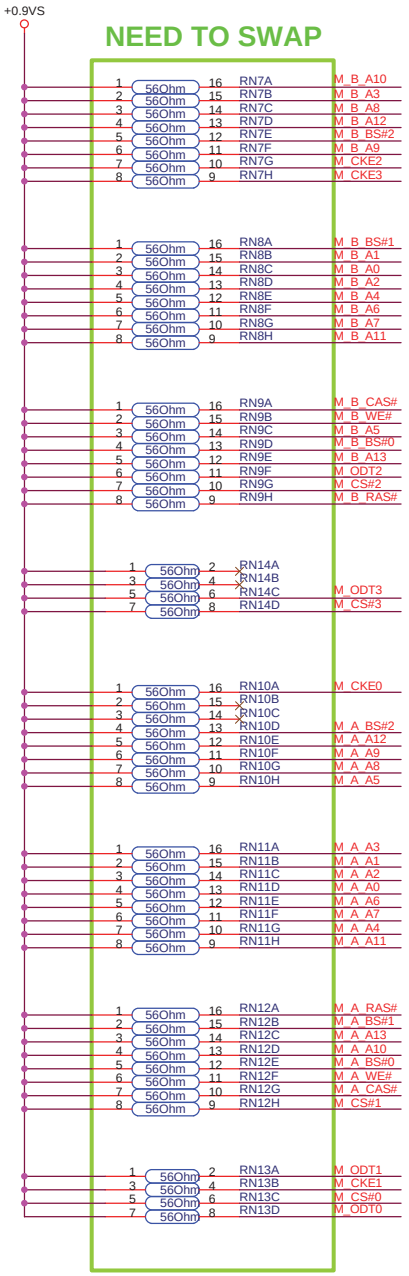




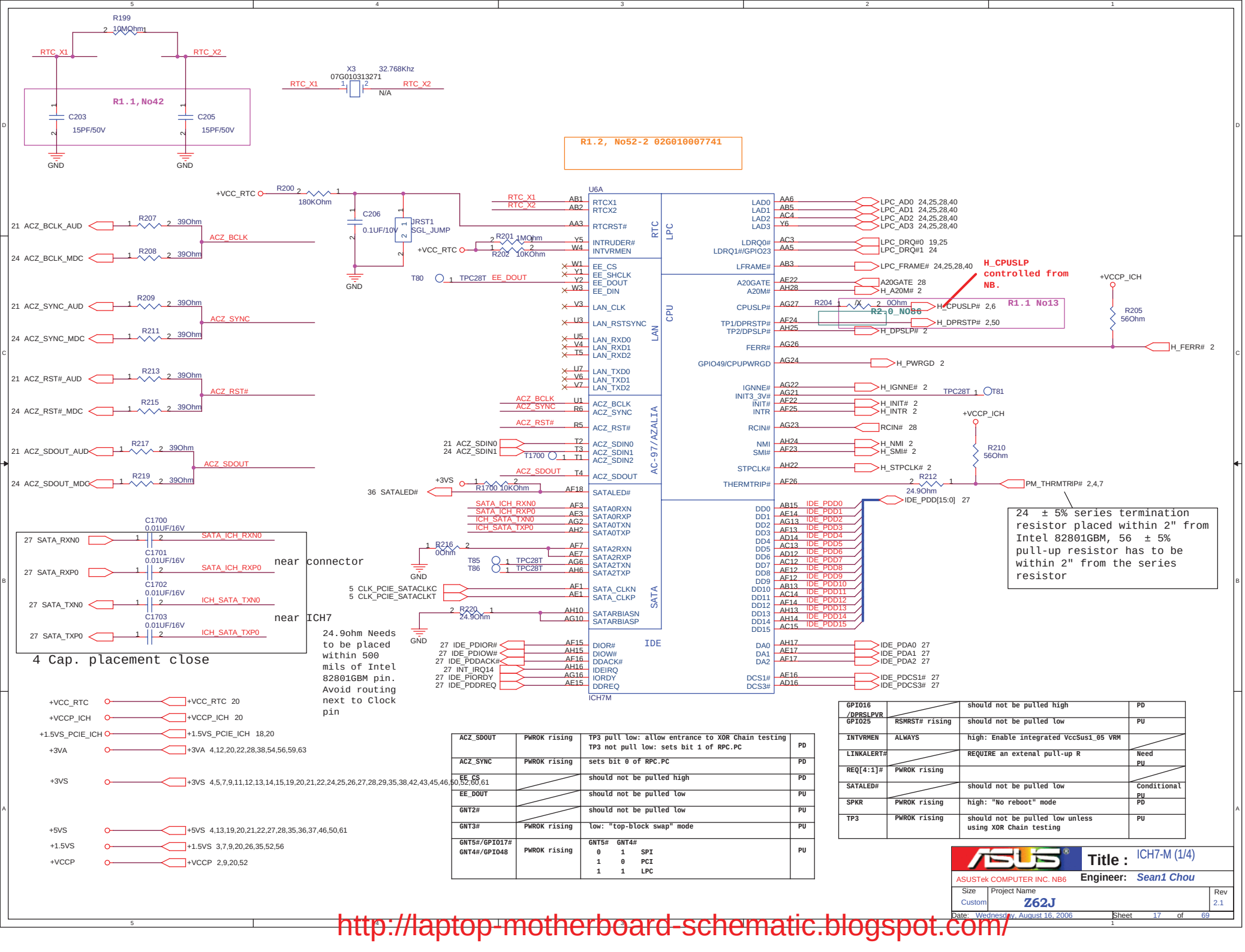
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS







ASUSTek COMPUTER INC. NB6	Title : DDR2 TERM	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 16 of 69	



ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

ASUSTek COMPUTER INC. NB6

Title : ICH7-M (1/4)

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 17 of 69

DEVICE	IDSEL	REQ/GNT	INT
LAN	AD23	REQ2#/GNT2#	INT A#
CARDBUS	AD17	REQ1#/GNT1#	INT B#, INT C#, INT D#

Internal					
SM Bus	INTB#	EIP	INTA#	PCIE6	INTB#
SATA	INTB#	U3P	INTD#	PCIE5	INTA#
PATA	INTA#	U2P	INTC#	PCIE4	INTD#
AC97 Modem	INTB#	U1P	INTB#	PCIE3	INTC#
		U0P	INTA#	PCIE2	INTB#
AC97 Audio	INTA#	HD Audio	INTA#	PCIE1	INTA#

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

Do not connect to reset on PCI slots or PCI down devices.

Pull-ups must be placed within 500 mils from Intel 82801GBM pins

ASUSTek COMPUTER INC. NB6	Title : ICH7-M (2/4)	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 18 of 69	

GPIO:
[0,6,7,16:23,32:39,48] - 3.3V core,
[1:5] - 5V core,
[8:15,24:31] - 3.3V resume,
[40:47] - N/A
[49] - V_CPU_IO

0 needs to check power plane again

For PCI compliance, SMBus signals should be routed to either all or none of the PCI slots in a chassis.
These signals should not be connected to SMLINK

checklist suggests +3V

R1.2, No49

GPIO 10 - Default GPI, 3.3V Resume

If ICH7M embedded Lan controller was used, "LAN_RST#" should be connected to "RSMRST#"

R2.0 NO86

PCB_VID3 : PROJECT CODE

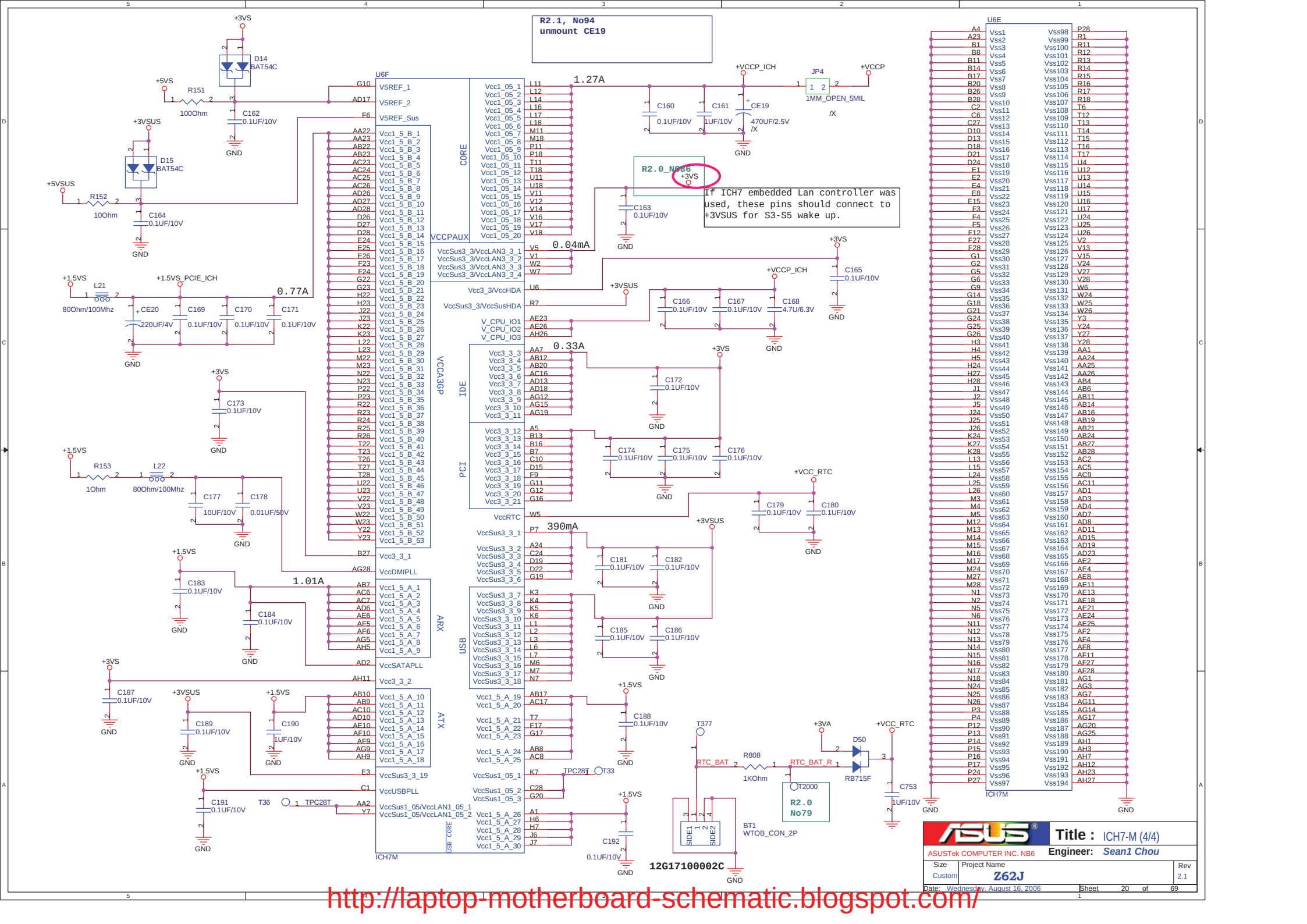
PCB_VID	0	1	2
MB V1.0	0	0	0
MB V1.1	0	0	1

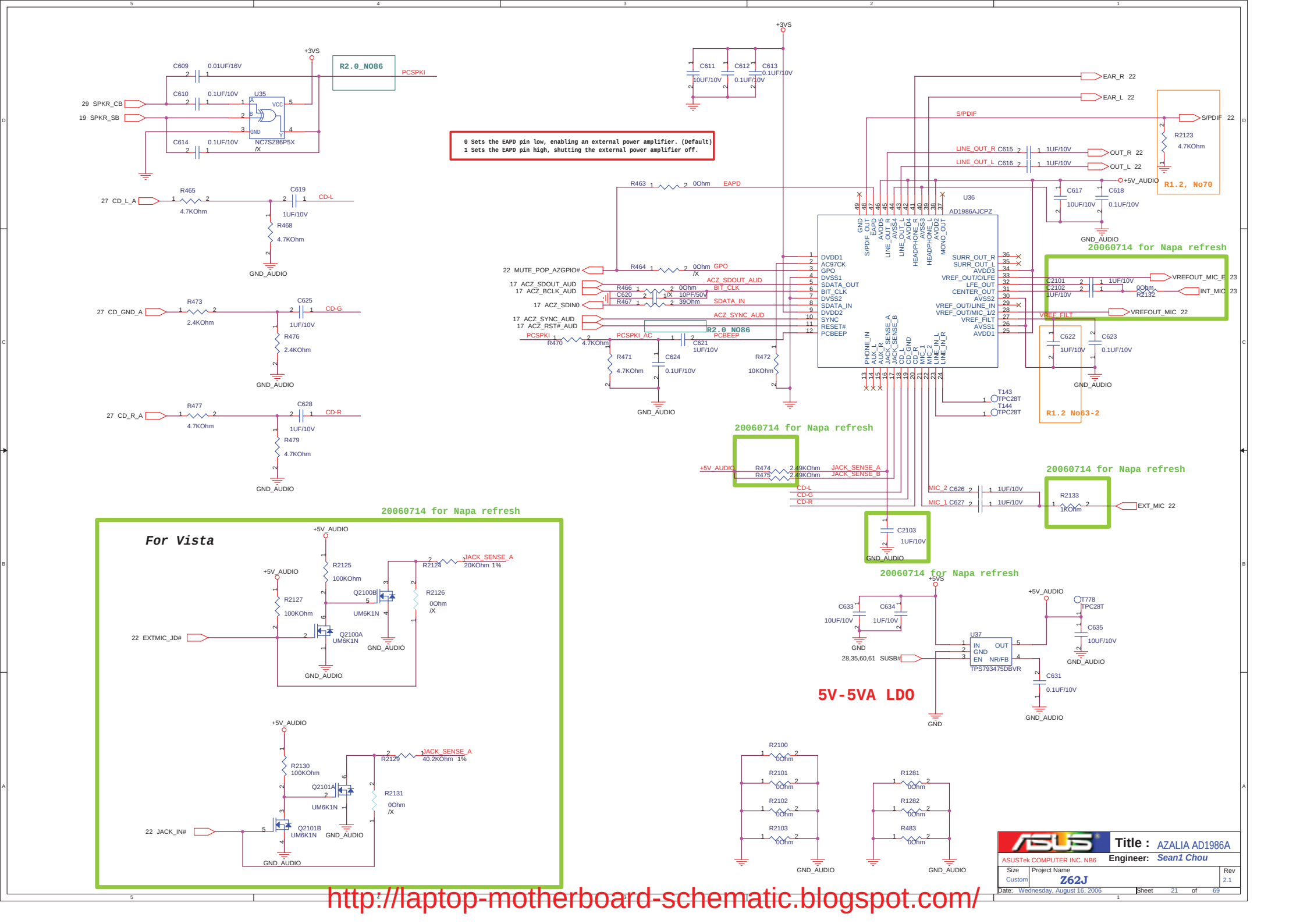
R1.1,No41

internal pull up

internal pull down

Title :	ICH7-M (3/4)
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou
Size: Custom	Project Name: Z62J
Rev: 2.1	
Date: Wednesday, August 16, 2006	Sheet 19 of 69


R2.1, No94
unmount CE19
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
R2.0 No86
1.27A
0.04mA
0.33A
0.77A
1.01A
390mA
U6F
U6E
ICH7M
Title : ICH7-M (4/4)
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Size: Custom
Project Name: Z62J
Rev: 2.1
Date: Wednesday, August 16, 2006
Sheet 20 of 69
12G17100002C
http://laptop-motherboard-schematic.blogspot.com/


+3VS
C609 0.01UF/16V
C610 0.1UF/10V
C614 0.1UF/10V
U35
NC7SZ86P5X
/X
R2.0_NO86
PCSPKI
29 SPKR_CB
19 SPKR_SB
0 Sets the EAPD pin low, enabling an external power amplifier. (Default)
1 Sets the EAPD pin high, shutting the external power amplifier off.
C611 10UF/10V
C612 0.1UF/10V
C613 0.1UF/10V
EAR_R 22
EAR_L 22
S/PDIF
S/PDIF 22
R2123 4.7KOhm
R1.2, No70
LINE_OUT_R C615 1UF/10V
LINE_OUT_L C616 1UF/10V
OUT_R 22
OUT_L 22
+5V_AUDIO
C617 10UF/10V
C618 0.1UF/10V
GND_AUDIO
R463 0Ohm EAPD
U36
AD1986AJCPZ
22 MUTE_POP_AZGPIO#
R464 0Ohm GPO
/X
17 ACZ_SDOUT_AUD
17 ACZ_BCLK_AUD
R466 0Ohm
C620 10PF/50V
R467 39Ohm
ACZ_SDOUT_AUD
BIT_CLK
SDATA_IN
17 ACZ_SDIN0
17 ACZ_SYNC_AUD
17 ACZ_RST#_AUD
ACZ_SYNC_AUD
R2.0_NO86
PCSPKI
R470 4.7KOhm
PCSPKI_AC
C621 1UF/10V
PCBEEP
R471 4.7KOhm
C624 0.1UF/10V
R472 10KOhm
20060714 for Napa refresh
SURR_OUT_R
SURR_OUT_L
VREF_OUT/C/LFE
LFE_OUT
CENTER_OUT
VREF_OUT/LINE_IN
VREF_OUT/MIC_1/2
VREF_FILT
C2101 1UF/10V
C2102 1UF/10V
0Ohm R2132
VREFOUT_MIC_E 23
INT_MIC 23
VREFOUT_MIC 22
VREF_FILT
C622 1UF/10V
C623 0.1UF/10V
R1.2 No53-2
T143 TPC28T
T144 TPC28T
20060714 for Napa refresh
+5V_AUDIO
R474 2.49KOhm
R475 2.49KOhm
JACK_SENSE_A
JACK_SENSE_B
CD-L
CD-G
CD-R
MIC_2 C626 1UF/10V
MIC_1 C627 1UF/10V
R2133 1KOhm
EXT_MIC 22
C2103 1UF/10V
20060714 for Napa refresh
+5VS
C633 10UF/10V
C634 1UF/10V
U37
TPS793475DBVR
28,35,60,61 SUSB#
T778 TPC28T
C635 10UF/10V
C631 0.1UF/10V
5V-5VA LDO
R2100 0Ohm
R2101 0Ohm
R2102 0Ohm
R2103 0Ohm
R1281 0Ohm
R1282 0Ohm
R483 0Ohm
R465 4.7KOhm
C619 1UF/10V
27 CD_L_A
CD-L
R468 4.7KOhm
R473 2.4KOhm
C625 1UF/10V
27 CD_GND_A
CD-G
R476 2.4KOhm
R477 4.7KOhm
C628 1UF/10V
27 CD_R_A
CD-R
R479 4.7KOhm
20060714 for Napa refresh
For Vista
+5V_AUDIO
R2125 100KOhm
R2127 100KOhm
Q2100B UM6K1N
Q2100A UM6K1N
R2126 0Ohm /X
R2124 20KOhm 1%
JACK_SENSE_A
22 EXTMIC_JD#
R2130 100KOhm
Q2101A UM6K1N
Q2101B UM6K1N
R2131 0Ohm /X
R2129 40.2KOhm 1%
22 JACK_IN#
ASUSTek COMPUTER INC. NB6
Title : AZALIA AD1986A
Engineer: Sean1 Chou
Size Custom
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 21 of 69
http://laptop-motherboard-schematic.blogspot.com/

SPEAKER CONN.

R1.1 No44
CHANGE P/N

SPKR+_MB_A — L31 220Ohm — SPKR+_MB_CON_A
SPKR-_MB_A — L32 220Ohm — SPKR-_MB_CON_A
SPKL+_MB_A — L33 220Ohm — SPKL+_MB_CON_A
SPKL-_MB_A — L34 220Ohm — SPKL-_MB_CON_A

U12 WtoB_CON_4P

12G171000047

SPEAKER is 4 ohm +- 15% / 2W /79 +- 3db (美星電子)
P/N:04-170003610

R1.1 No37
C2201 150PF/50V /X
C2202 150PF/50V /X
C2203 150PF/50V /X
C2204 150PF/50V /X

HEADPHONE JACK

21 EAR_L
21 EAR_R
21 JACK_IN#
S/PDIF 21
+5VS
+VAMP
C307 0.1UF/10V
R269 10KOhm
R1266 0Ohm
C1074 100PF/50V /X
EAR_L_O R1267 22Ohm
EAR_R_O R1268 22Ohm
No2.1, No96
C305 100PF/50V
C306 100PF/50V
J1 SW 0N9
PHONE_JACK_8P

12G140001089

AUDIO OUT AMP

+5VS
+VAMP
U13 TPA0212PWPRG4
GAIN0_MB
GAIN1_MB
SPKL+_MB_A
SPKL-_MB_A
SPKR+_MB_A
SPKR-_MB_A
SE/BTL#
OP_SD#
21 OUT_L
OUT_R 21
R266 30KOhm
R265 30KOhm
R2.0, No81
C301 1UF/10V
C300 1UF/10V
C302 0.47UF/16V
C303 0.47UF/16V
C304 0.47UF/16V
R262 0Ohm
R264 0Ohm
GND_AUDIO

GAIN0	GAIN1	SE/BTL#	AV (V/V)
0	0	0	-2
0	1	0	-6
1	0	0	-12
1	1	0	-24
X	X	1	-1

R1.2, No53
R261 10KOhm
R263 0Ohm /X
R2201 10KOhm /X
R2202 0Ohm
C297 10UF/10V
C298 0.1UF/10V
C299 1UF/10V
Close to OP

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.

Vista UAA driver will set this pin low as default, so it needs inverted.

21 MUTE_POP_AZGPIO#
MUTE_POP
DLY_OP_SD#
Q2200 2N7002
D23 1N4148W
Z62JM ER NO1

+12VS
+5V
+3VS
R270 1MOhm
D2200 1N4148W
R271 470KOhm
R272 10KOhm
Q19A UM6K1N
Q19B UM6K1N
Q20B UM6K1N
Q20A UM6K1N
Q21A UM6K1N
Q21B UM6K1N
EAR_R
EAR_L
EAR_R_C
EAR_L_C
AMP_RST#
C2205 0.1UF/25V
Z62JM ER NO2
Solve pop noise

But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.

R1257 10KOhm
SE/BTL#
Q22A UM6K1N
Q22B UM6K1N
JACK_IN#
C2206 2.2UF/6.3V
Z62JM ER NO5

R1.1 No31

Colay:
330 uF for Vista

20060714 for Napa refresh

CE7000 330UF/6.3V
CE21 47UF/6.3V /X
CE22 47UF/6.3V /X
CE7001 330UF/6.3V
RN16A 1KOhm
RN16B 1KOhm

$$f(highpass)=\frac{1}{2*3.14*R*C}=73$$

R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.

+3VA
28 OP_SD#
D24 1N4148W
R275 10MOhm
R276 10KOhm
C308 0.1UF/10V
U82A SN74LV14APWR
U82B SN74LV14APWR
DLY_OP_SD 4
DLY_OP_SD#

20060714 for Napa refresh

VREFOUT_MIC 21
21 EXT_MIC
21 EXTMIC_JD#
R2203 3KOhm
L7000 220Ohm
L35 1KOhm/100Mhz
J2 AUDIO JACK PHONE_JACK_6P
C2200 100PF/50V
D7000 EGA10603V05A1 /X
D7001 EGA10603V05A1 /X
C7370 1000PF/50V /X

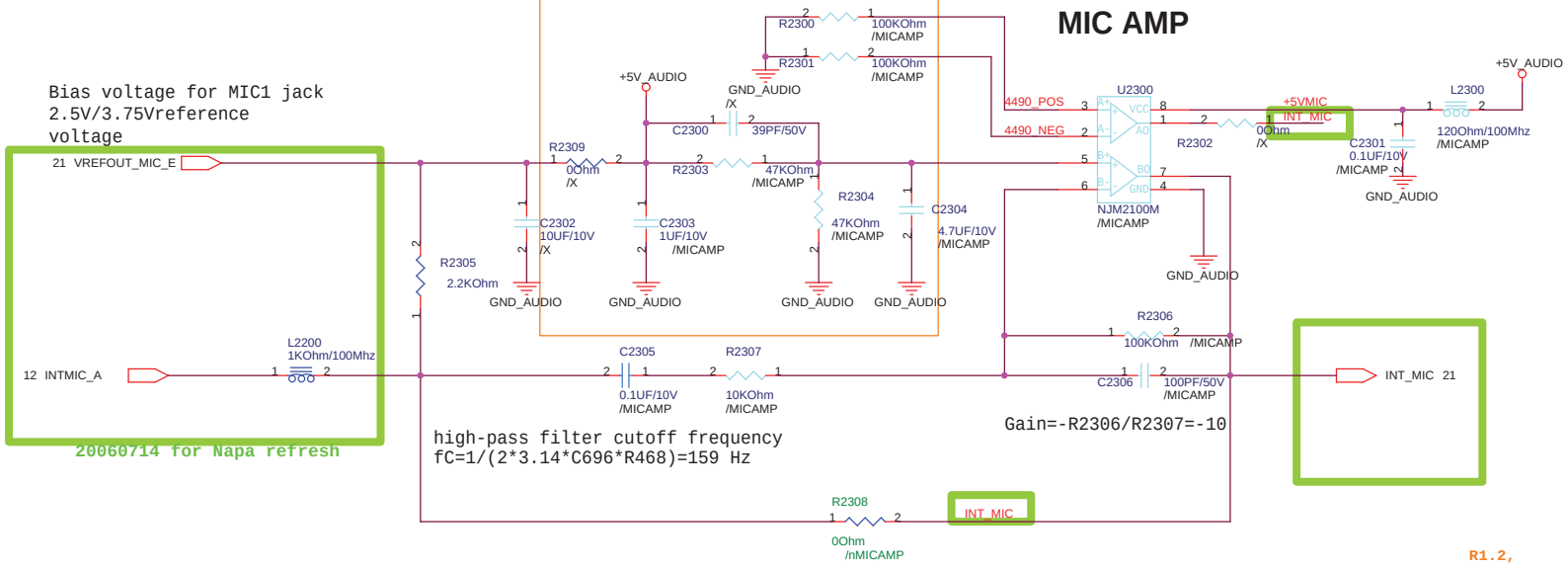
12G14030106L
PIN2 and PIN6 normal close
PIN4 and PIN5 normal open

External Microphone

ASUSTek COMPUTER INC. NB6	Title : AUDIO AMP	
	Engineer: Sean1 Chou	
Size: C	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 22 of 69	

R1.2, No63

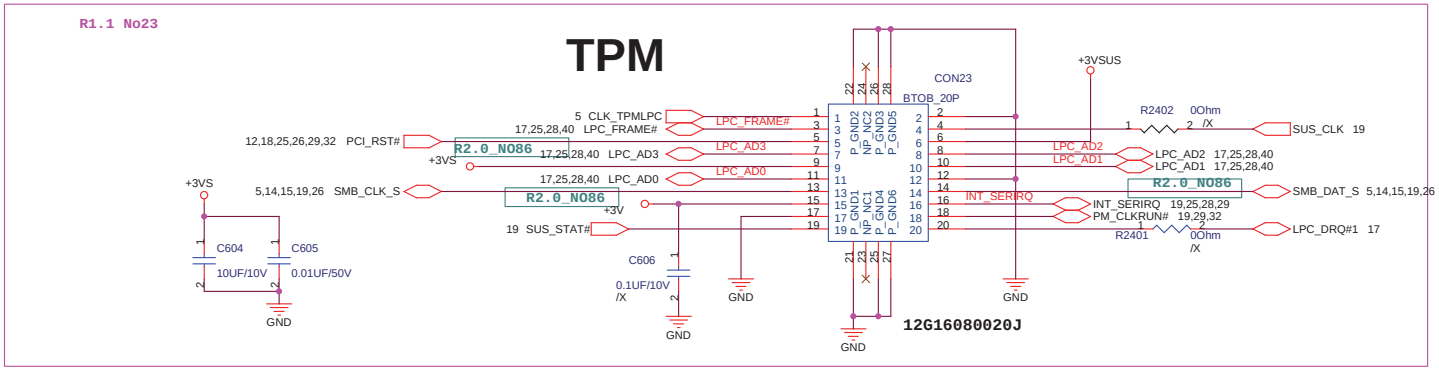
ADI suggests:
1. No install C2300
2. No install C2302
3. Ground bottom of R2304
4. Change R2303, R2304 to 47K. Change C2304 to 4.7uF
5. C2305 should be 0.1uF
6. Suggest using 100pF for C2306

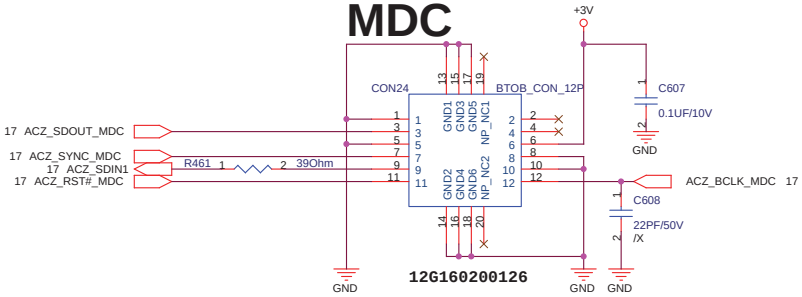


R1.2,
No50-1

ASUSTek COMPUTER INC. NB6	Title : MIC Pre-AMP	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 23 of 69	

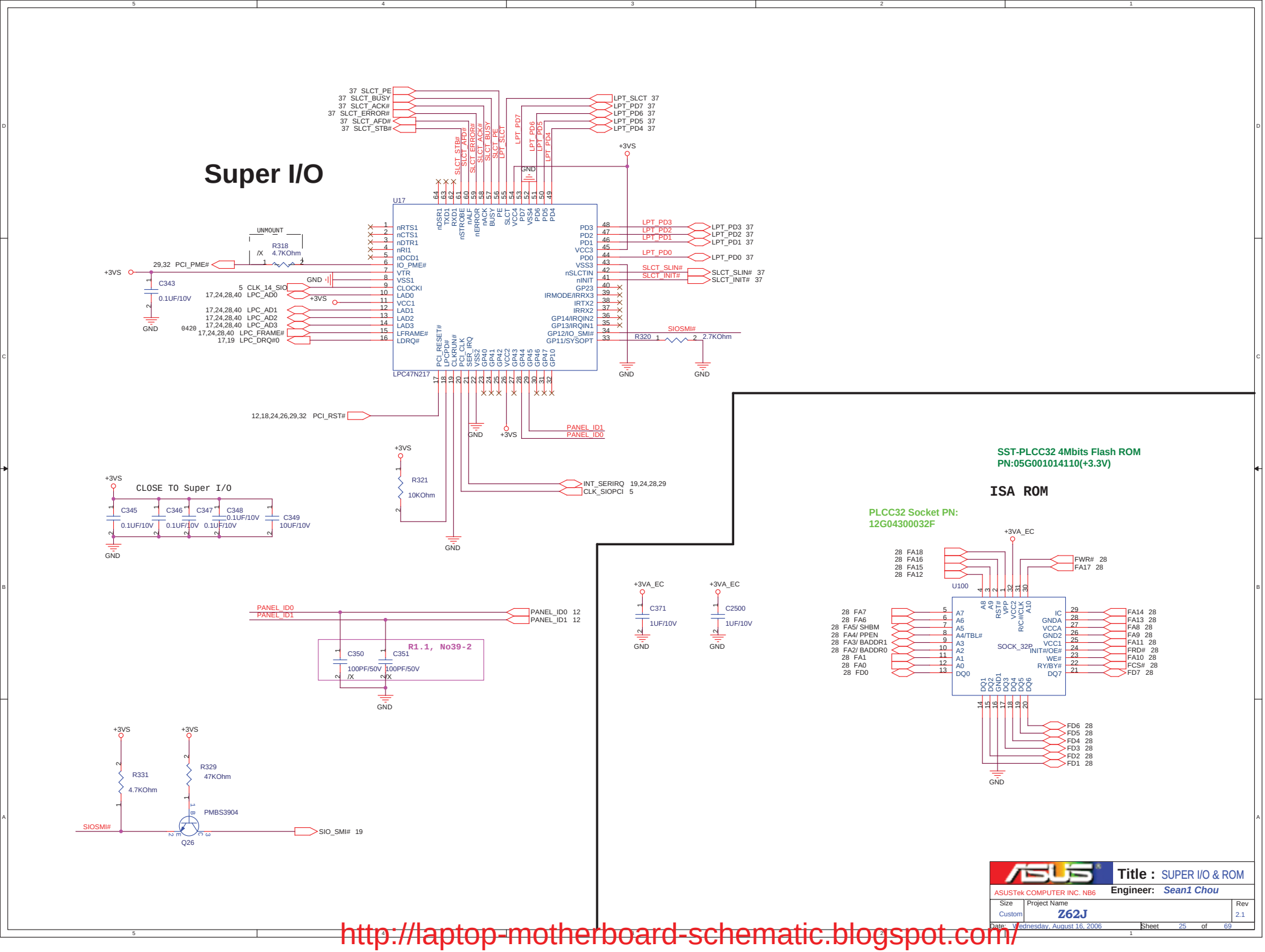
R1.1 No23





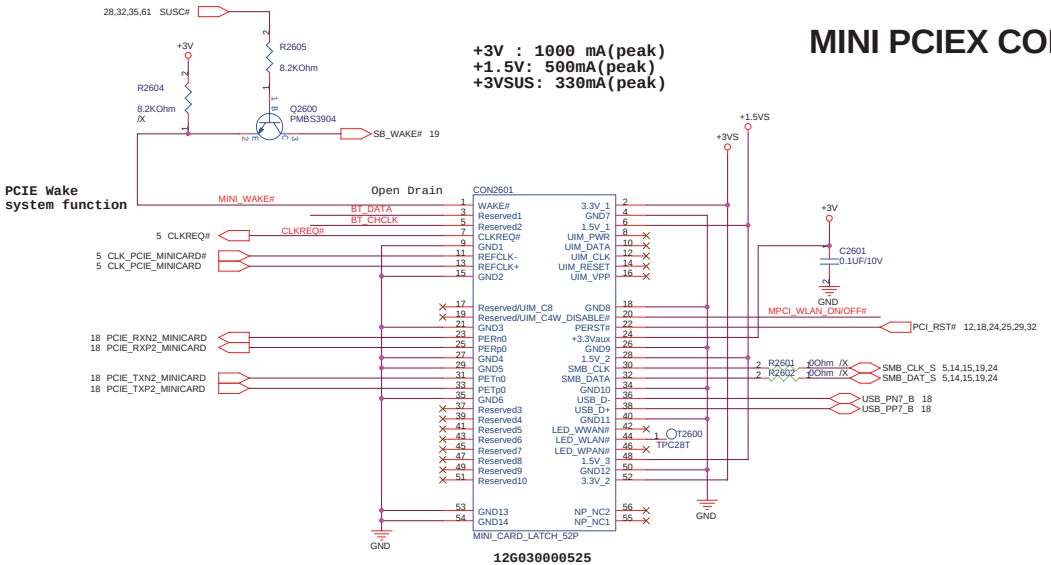
LPC CLK	Pin # 1	Pin # 2	GND
LPC_FRAME#	3	4	NC
RESET#	5	6	NC
LPC_AD3	7	8	LPC_AD2
+3VS	9	10	LPC_AD1
LPC_AD0	11	12	GND
NC	13	14	NC
+3V	15	16	SERIRQ
GND	17	18	CLKRUN#
LPC_PD#	19	20	NC

ASUSTek COMPUTER INC. NB6	Title : MODULE-TPM/MDC		
	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 24 of 69		

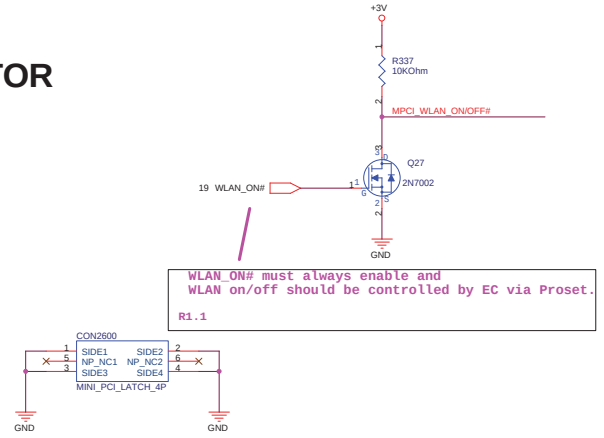


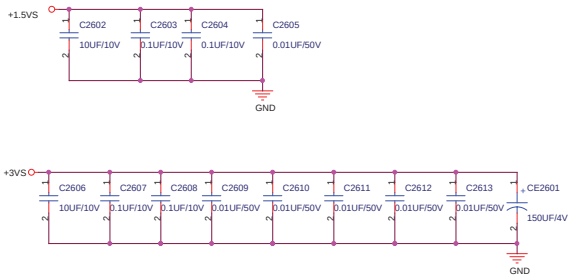
MINI PCIEX CONNECTOR

+3V : 1000 mA(peak)
+1.5V: 500mA(peak)
+3VSUS: 330mA(peak)

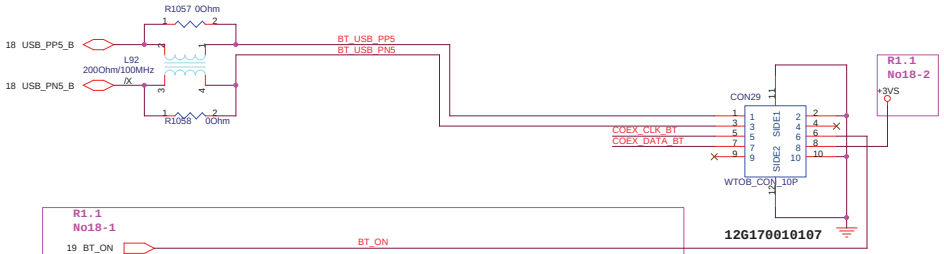


12G030000525





BLUETOOTH CONNECTOR

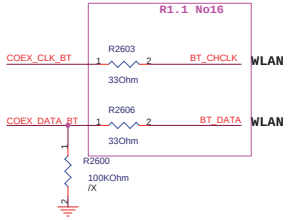


12G170010107

Check O/D output or push pull

Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT

BT_ON 3.3V at GPIO38



BT Module has no leakage, so discard PMOS block circuits

Title : MINI PCIEX (TV) & BT Conn		
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou	
Size: C	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 26 of 69	

For Z62J, SATA HDD plug-in is reversed, so the pin definition is reversed.

+3VS
R339 2 1 4.7KOhm IDE_PIORDY
R340 1 2 8.2KOhm INT_IRQ14
+5VS
R341 1 2 10KOhm IDE_DIAG

+5VS
R343 10KOhm
R344 10KOhm
if use EC ->3V
IDE_RST#
Q28B UM6K1N
Q28A UM6K1N
7,18,19,28,42 PLT_RST#
GND GND

+5VS
CE2701 10UF/10V
CE2702 10UF/10V
C2700 4700PF/25V
C2701 4700PF/25V
GND

+3VS
CE2703 10UF/10V
C2702 4700PF/25V
GND

17 SATA_TXP0
17 SATA_TXN0
17 SATA_RXN0
17 SATA_RXP0
+3VS
+5VS
GND

CON2700
P_GND2 26
NP_NC2 24
NP_NC1 23
P_GND1 25
SATA_CON_22P
GND
12G151100229

SATA HDD

CD-ROM

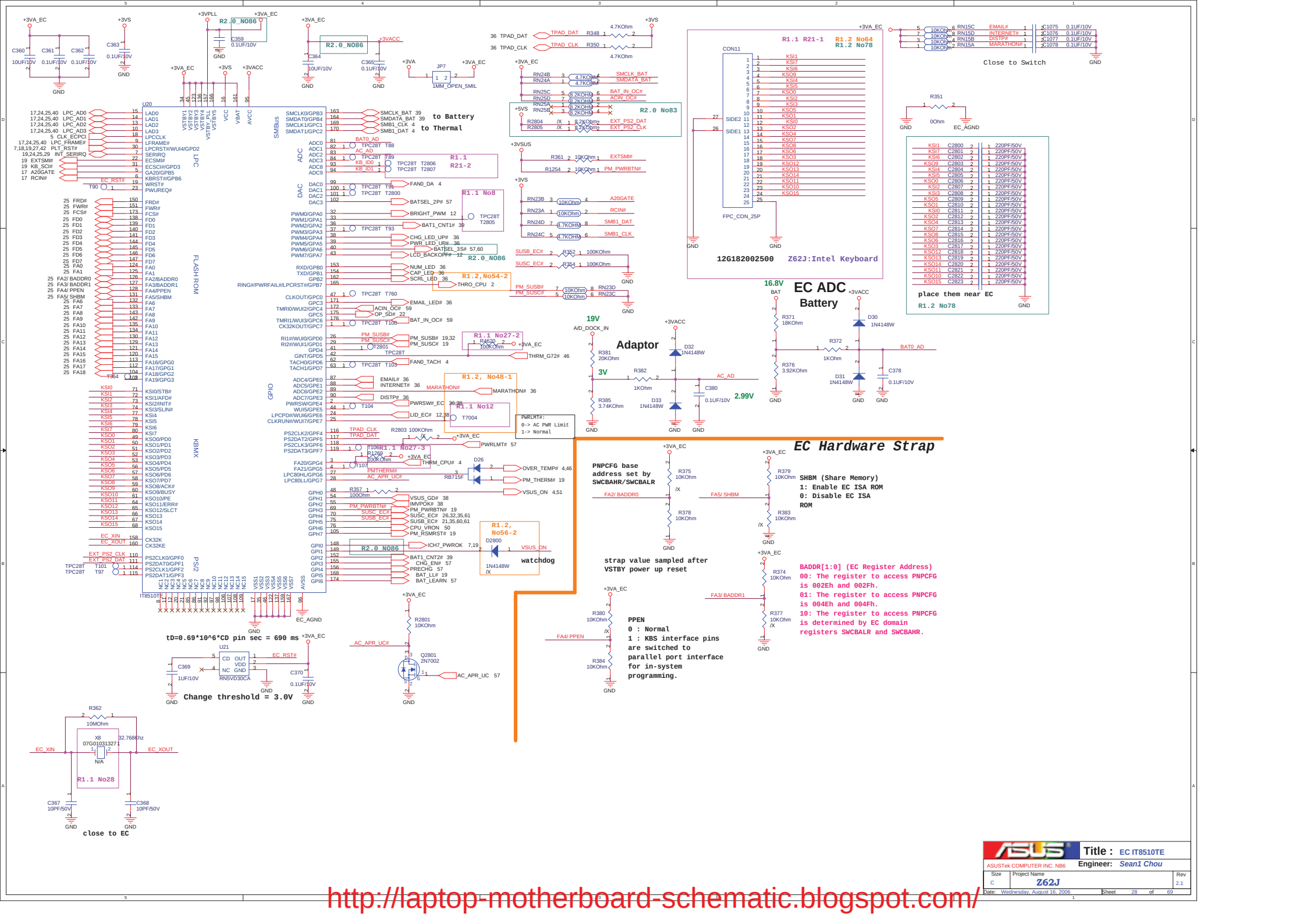
+5VS
ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master
R345 1 2 470Ohm /X ODD_CSEL
R346 1 2 470Ohm
GND
R2.1, No90
to set CDROM master

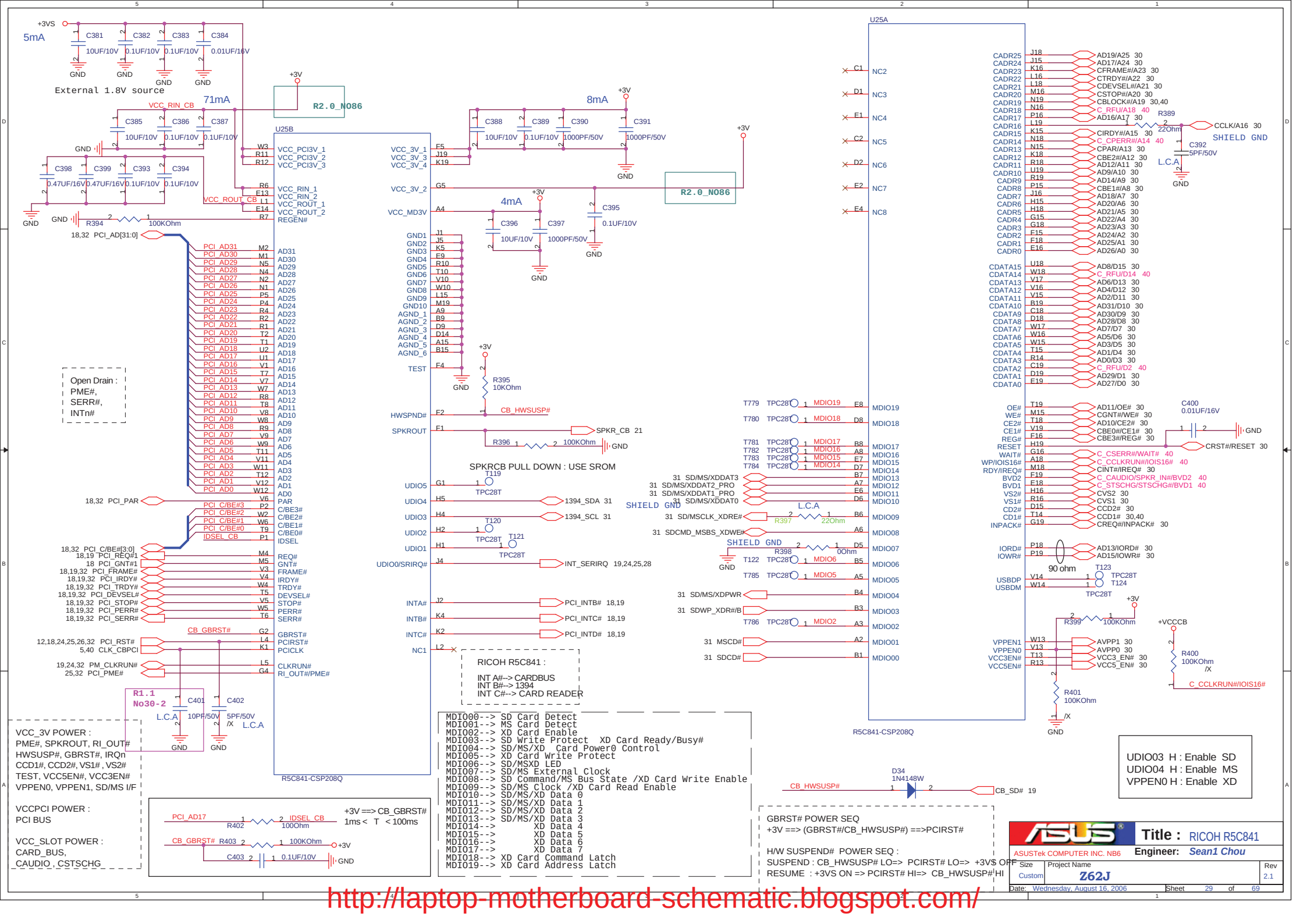
+5VS
R2701 1 2 10KOhm IDE_IOCS16_2#

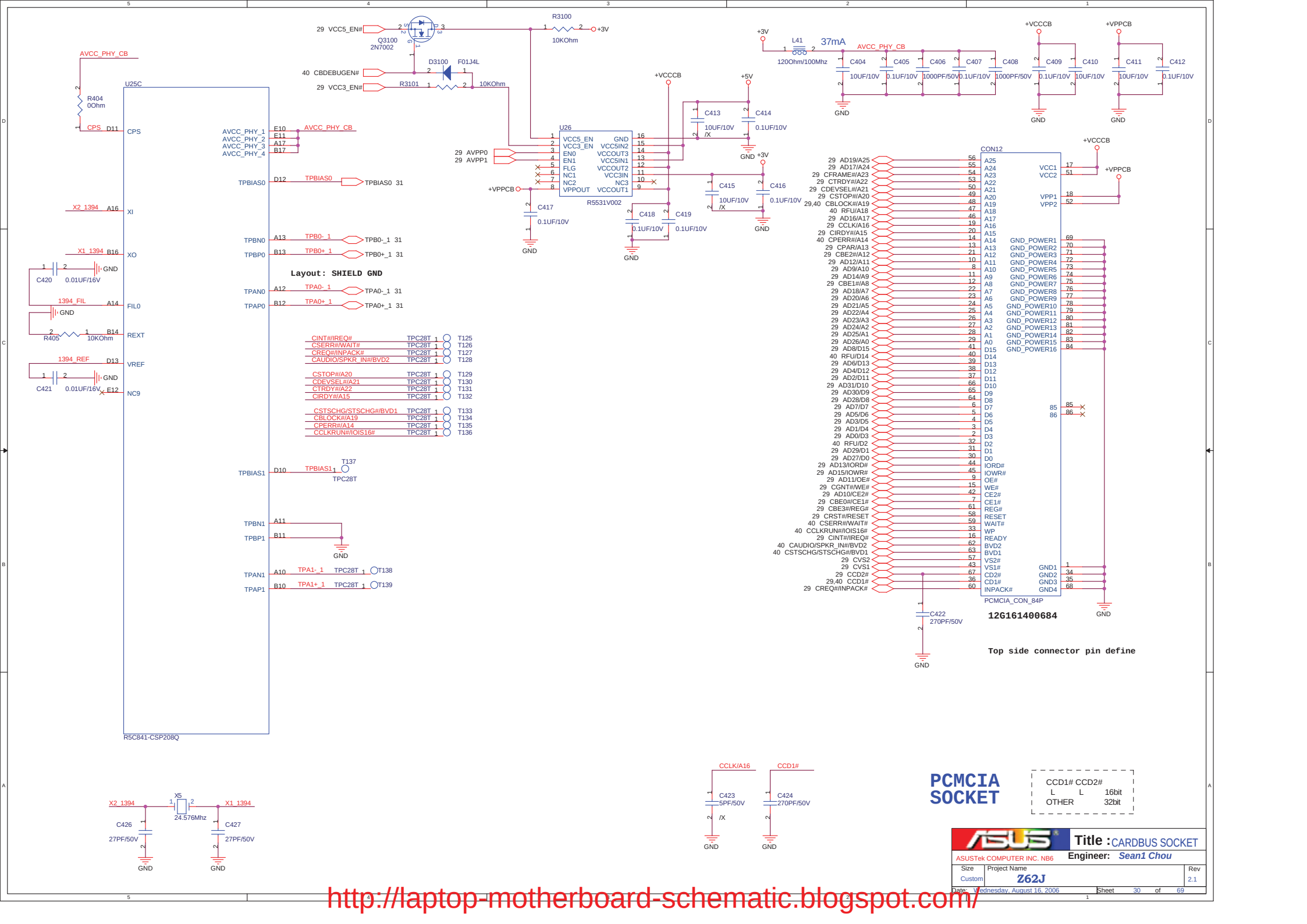
17 IDE_PDD[15:0]
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15

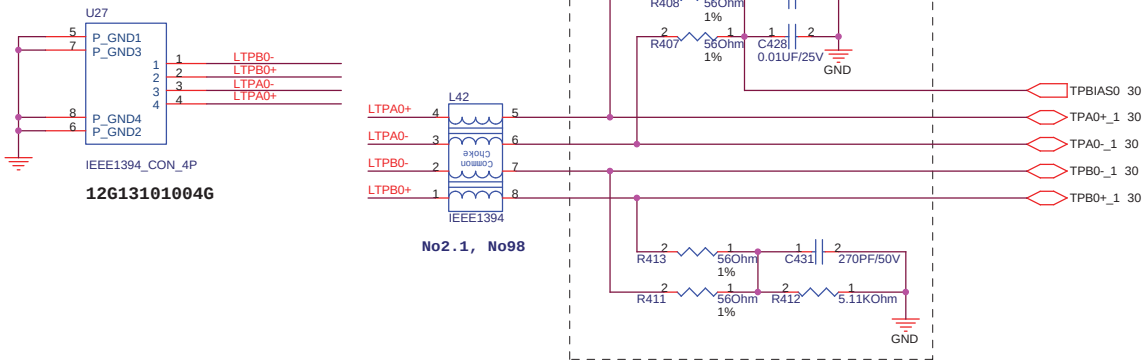
R1.1, No36
CON10
NP_NC3 NP_NC4 NP_NC2
21 CD_L_A
21 CD_GND_A
CD_R_A 21
CD_GND_A
IDE_RST#
IDE_PDD7
IDE_PDD6
IDE_PDD5
IDE_PDD4
IDE_PDD3
IDE_PDD2
IDE_PDD1
IDE_PDD0
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDDREQ
IDE_PDIOR#
17 IDE_PDIOW#
17 IDE_PIORDY
17 INT_IRQ14
17 IDE_PDA1
17 IDE_PDA0
17 IDE_PDCS1#
IDE_PDIOW#
IDE_PIORDY
INT_IRQ14
IDE_PDA1
IDE_PDA0
IDE_PDCS1#
IDE_PDDACK#
IDE_IOCS16_2#
IDE_DIAG
IDE_PDA2
IDE_PDCS3#
IDE_PDREQ 17
IDE_PDIOR# 17
IDE_PDDACK# 17
IDE_PDA2 17
IDE_PDCS3# 17
TPC28T
T2700
+5VS
ODD_CSEL
cd_rom_50p
GND GND
12G161210507
+5VS
CE24 10UF/10V
GND

ASUSTek COMPUTER INC. NB6	Title : HDD & CDROM	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 27 of 69	

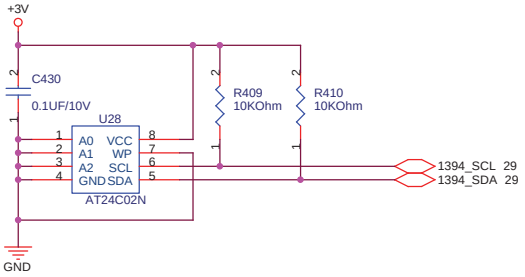


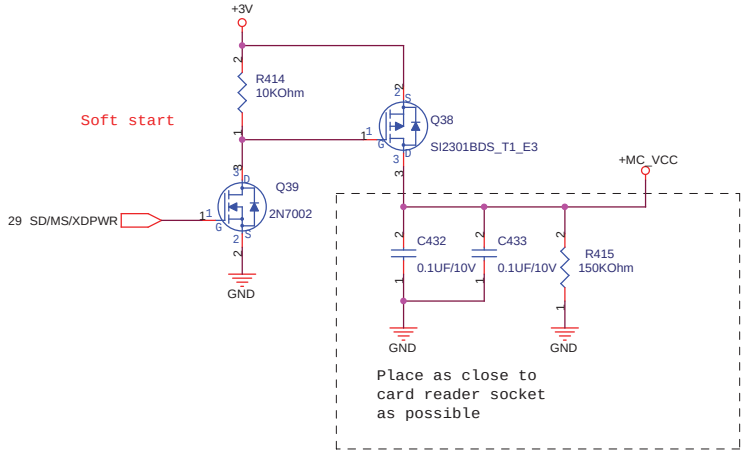


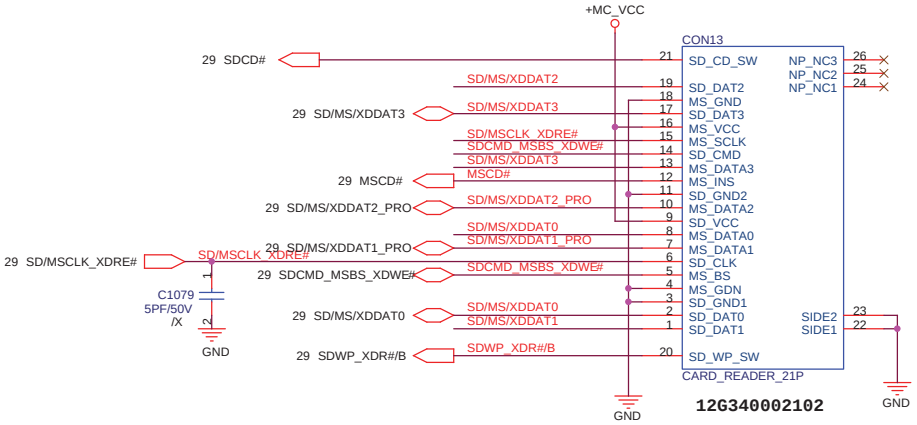




1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

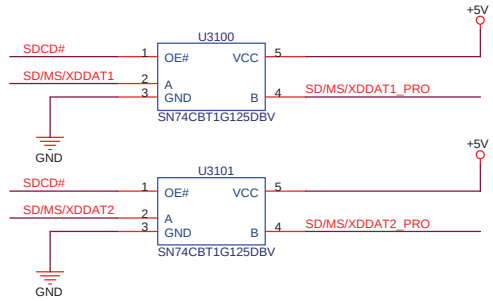






Layout: SHIELD GND

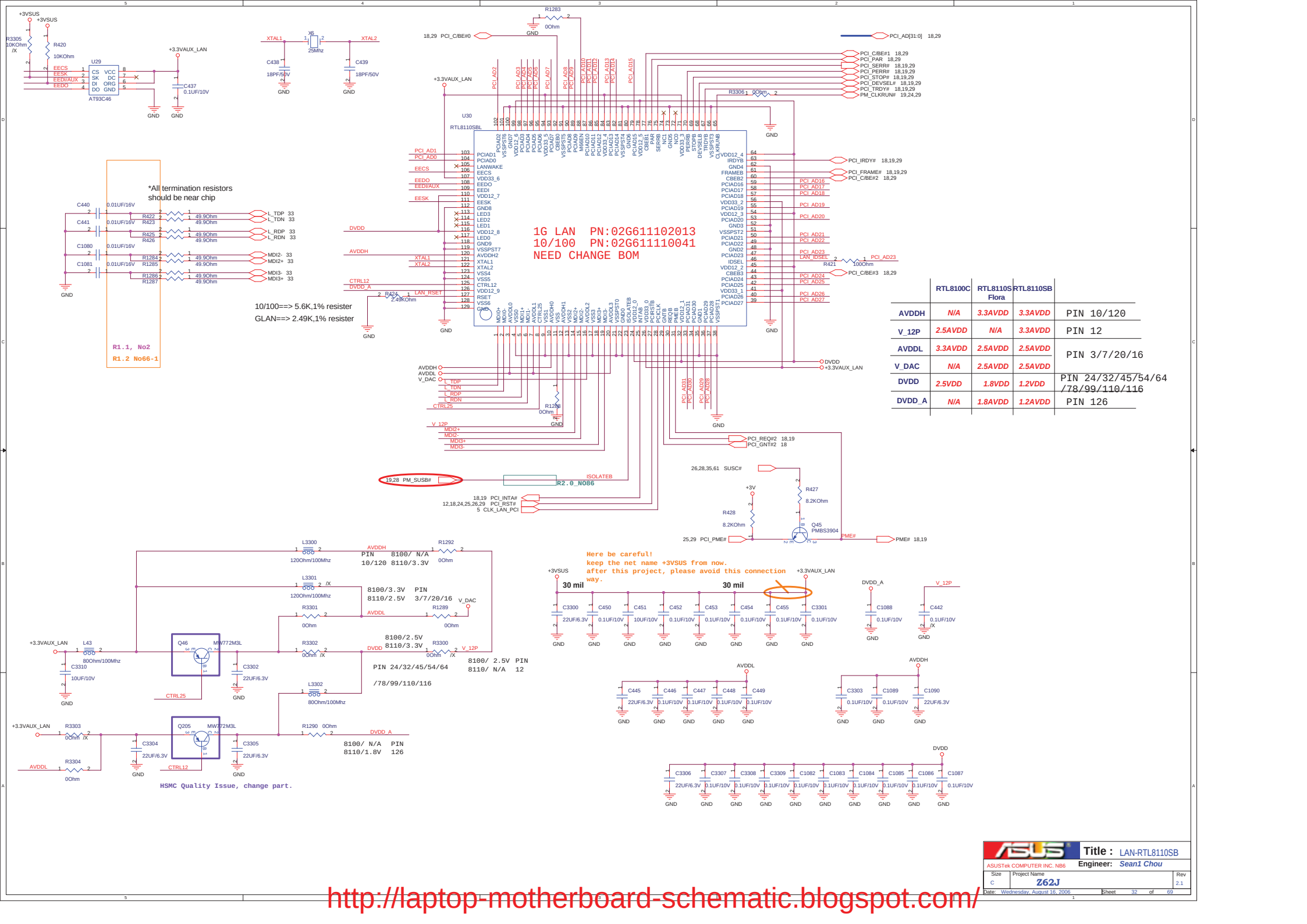
R1.0 No80



For correcting the isuue MS Duo adaptor plugging in

R1.1 No14

ASUSTek COMPUTER INC. NB6	Title : 1394 & 3 IN 1 CON	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 31 of 69	



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

Title :	LAN-RTL8110SB		
ASUSTek COMPUTER INC. NB6	Engineer:	Sean1 Chou	
Size: C	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 32 of 69		

LAN PORT

CON27
SIDE2 4
2
1
SIDE1 3
RJ11_RING_CON
RJ11_TIP_CON
WTOB_CON_2P
12G17000002B
1KOhm/100Mhz 1 2 L82
1KOhm/100Mhz 1 2 L83
C893 1000PF/3KV N/A GND
C894 1000PF/3KV N/A GND
R2.1, No89
CON28
RJ11_RING
RJ11_TIP
LAN_TXP
LAN_TXN
LAN_RXP
LAN_MDI2P
LAN_MDI2N
LAN_RXN
LAN_MDI3P
LAN_MDI3N
1 SIDE1 17
2 P_GND1 15
3 NP_NC1 13
10 NP_NC2 14
11 P_GND2 16
12 SIDE2 18
MODULAR_JACK_12P
12G142111121

R1.1 CAE change footprint

R1.2 No66-3

TRANSFORMER 10/100MB
Dual Layout with GiGa Transformer.

U3300
L_RDN 1 RD+ RX+ 16 LAN_RDN
L_RDP 2 RD- RX- 15 LAN_RDP
RDC1 3 RDCT RXCT 14 L_CMT1
RDC2 6 PTCT/TDCT XCT 11 L_CMT0
L_TDN 7 TD+ TX+ 10 LAN_TDN
L_TDP 8 TD- TX- 9 LAN_TDP
4 NC1 NC3 12
5 NC2 NC4 13
10/100MB
/X

L_RDP_MB 37
L_RDN_MB 37
L_TDP_MB 37
L_TDN_MB 37

R1293 unmount when using 10/100 LAN

AVDDL
R1293 0Ohm
RDC
32 MDI3-
32 MDI3+
32 MDI2-
32 MDI2+
R3311 0Ohm
32 L_RDN
32 L_RDP
R3312 0Ohm
32 L_TDN
32 L_TDP

U60
TCT1 1
TD1+ 2
TD1- 3
TCT2 4
TD2+ 5
TD2- 6
RDC1 TCT3 7
TD3+ 8
TD3- 9
RDC2 TCT4 10
TD4+ 11
TD4- 12
1GB

24 MCT1 L_CMT3
23 MX1+ LAN_MDI3- LAN_MDI3- 37
22 MX1- LAN_MDI3+ LAN_MDI3+ 37
21 MCT2 L_CMT2
20 MX2+ LAN_MDI2- LAN_MDI2- 37
19 MX2- LAN_MDI2+ LAN_MDI2+ 37
18 MCT3 L_CMT1
17 MX3+ LAN_RDN LAN_RDN 37
16 MX3-
15 MCT4 L_CMT0
LAN_RDP LAN_RDP 37
14 MX4+ LAN_TDN LAN_TDN 37
13 MX4- LAN_TDP LAN_TDP 37

C1091 0.01UF/25V
C1092 0.01UF/25V
C1093 0.01UF/25V
C1094 0.01UF/25V
GND

L_RDP_MB 1 0Ohm 2 RN45A LAN_RXP
L_RDN_MB 3 0Ohm 4 RN45B LAN_RXN
L_TDP_MB 5 0Ohm 6 RN45C LAN_TXP
L_TDN_MB 7 0Ohm 8 RN45D LAN_TXN

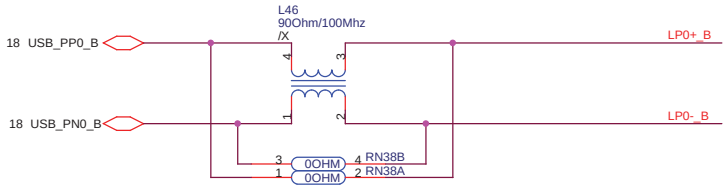
20060714 for Napa refresh

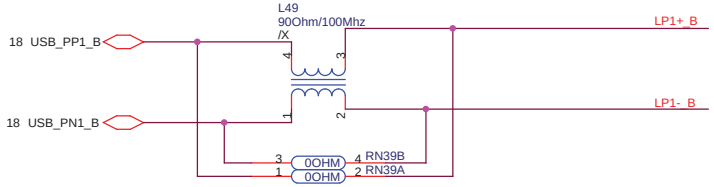
L_MDI2+_MB 1 0Ohm 2 RN47A LAN_MDI2P
L_MDI2-_MB 3 0Ohm 4 RN47B LAN_MDI2N
L_MDI3+_MB 5 0Ohm 6 RN47C LAN_MDI3P
L_MDI3-_MB 7 0Ohm 8 RN47D LAN_MDI3N

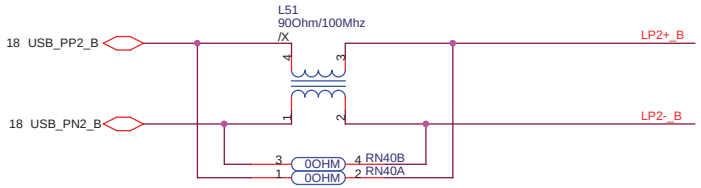
L_MDI3+_MB 37
L_MDI3-_MB 37
L_MDI2+_MB 37
L_MDI2-_MB 37

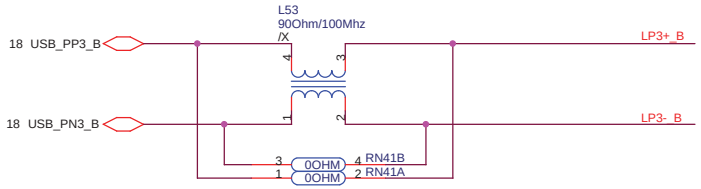
LAN_MDI3- R3307 75Ohm 1 2 /X GND_LAN
LAN_MDI3+ R3308 75Ohm 1 2 /X
LAN_MDI2- R3309 75Ohm 1 2 /X
LAN_MDI2+ R3310 75Ohm 1 2 /X
L_CMT0 RN46A 75Ohm 1 2
L_CMT1 RN46B 75Ohm 3 4
L_CMT2 RN46C 75Ohm 5 6
L_CMT3 RN46D 75Ohm 7 8
C769 0.1UF/10V

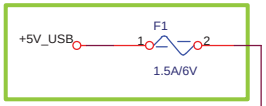
ASUSTek COMPUTER INC. NB6	Title : RJ11+45	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 33 of 69	

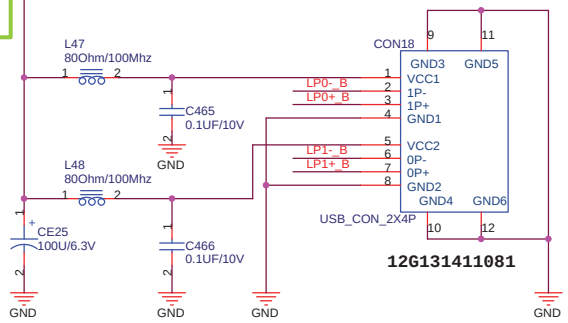




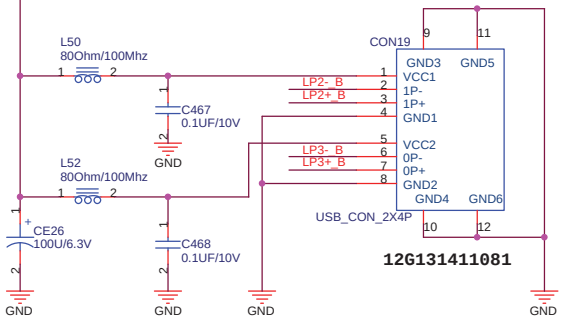








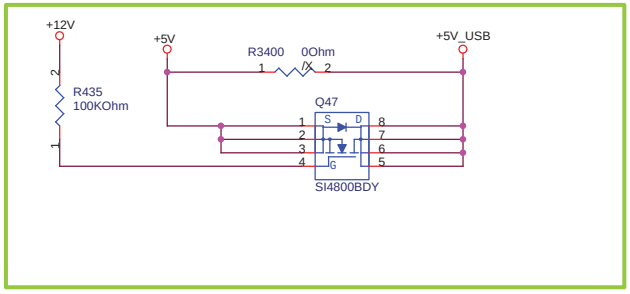
CAE modify: need check layout



Z62JM ER NO3

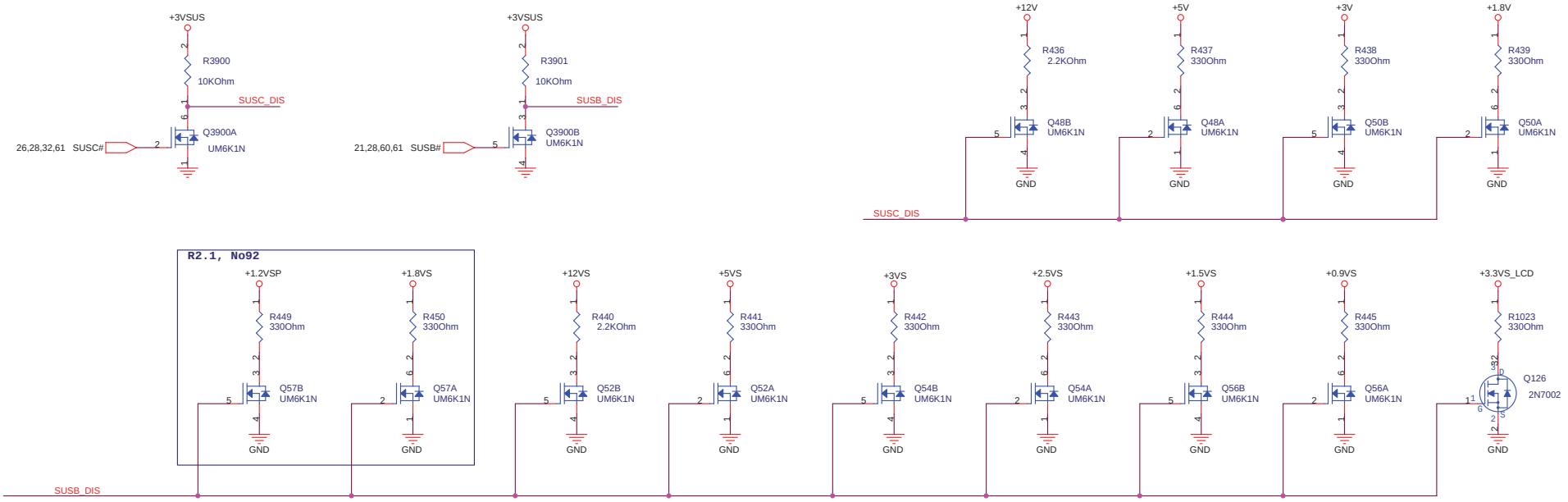
add back MOS to solve USB power leakage

R2.1, No93

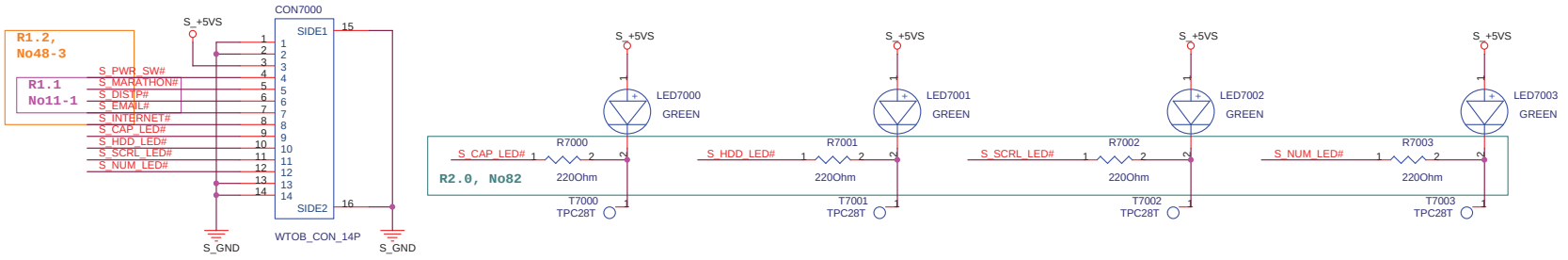


ASUSTek COMPUTER INC. NB6	Title : USB CONN X 5	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 34 of 69	

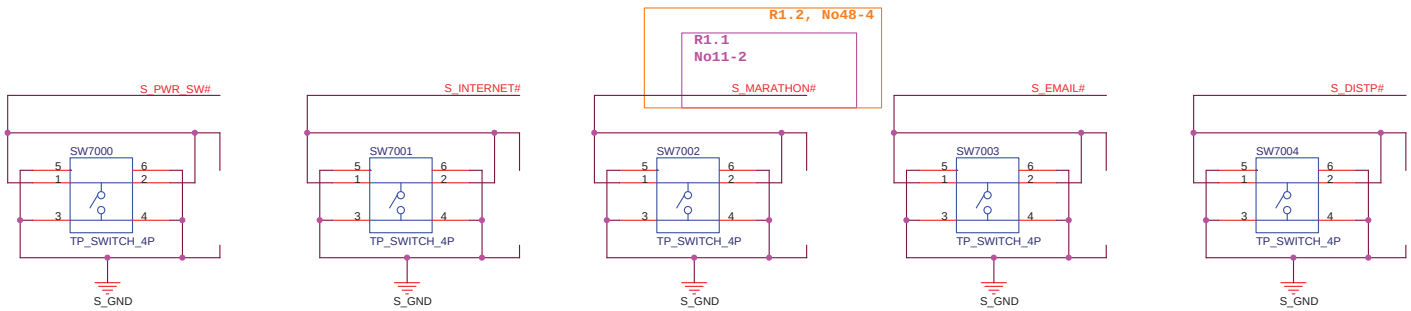
Discharge Circuit

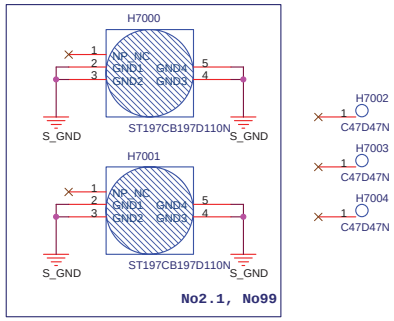


Launch Board

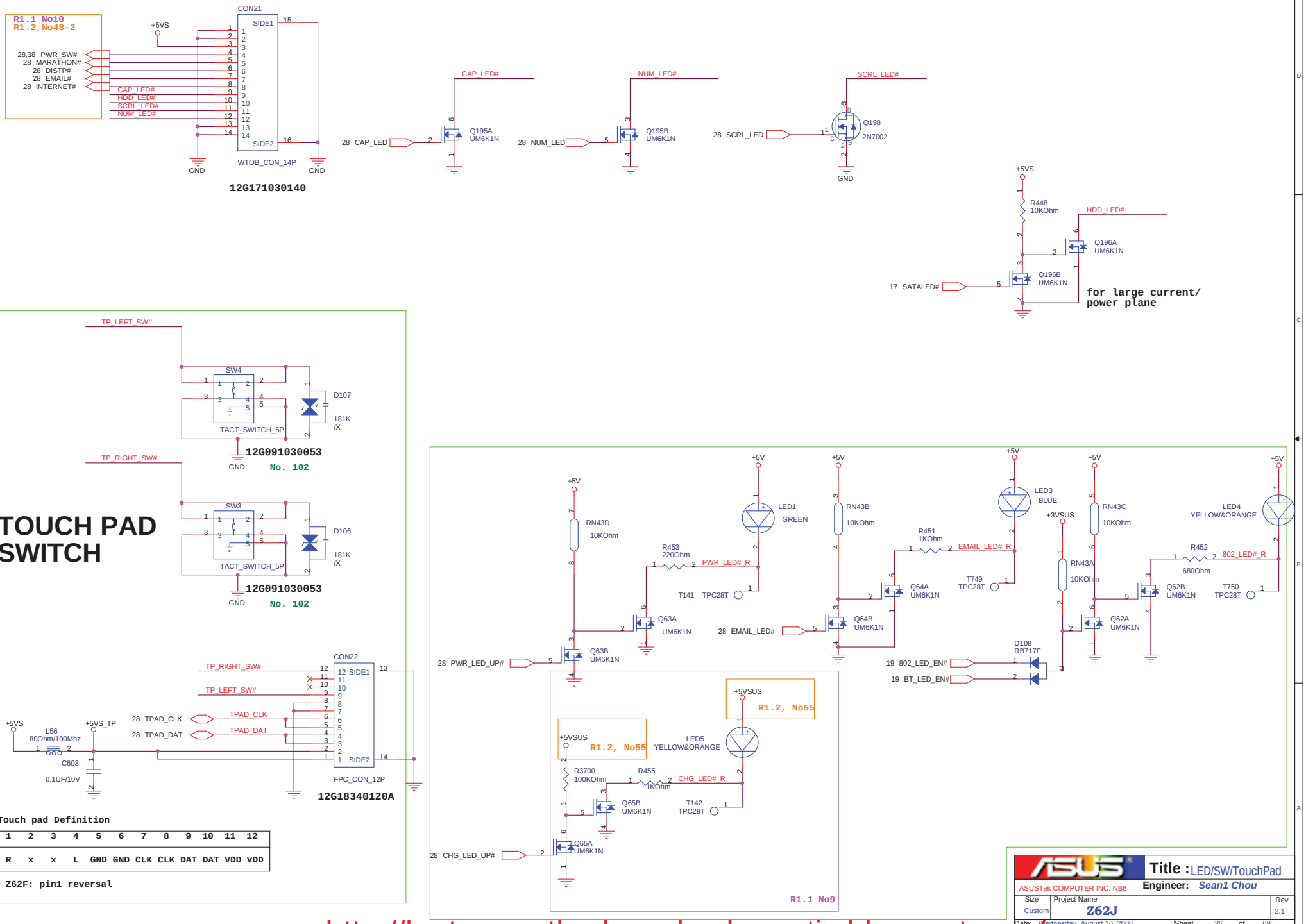


12G171030140





Title : Discharge Circuit & Launch B		
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 35 of 69	



if we use +3V, PR_IN will be low when entering S4,S5, and then switch to PortBar (can not wake on on-board LAN)

R1.2,No45

+3VSUS

PR_IN# pull high to make sure can switch to CRT.

R818 10KOhm

13 PR_IN#

PR_IN#

D56 1SS355

A/D_DOCK_PR

A/D_DOCK_IN

DOCK_VIN_P

L65 680Ohm/100Mhz

4 A(Typ)

Q71 SI3457BDV

R819 100KOhm

R820 20KOhm

PR_IN# Q

For EMI (NEAR CONNECTOR)

A/D_DOCK_PR

+5VS

+5V_PR

C771 0.1UF/25V

C772 0.1UF/10V

C773 0.1UF/10V

PORT BAR III CONN.

L_MDI2-_MB
L_MDI2+_MB
L_MDI3+_MB
L_MDI3-_MB

L_MDI2-_MB 33
L_MDI2+_MB 33
L_MDI3+_MB 33
L_MDI3-_MB 33

L_TDP_MB
L_TDN_MB
L_RDP_MB
L_RDN_MB

L_TDP_MB 33
L_TDN_MB 33
L_RDP_MB 33
L_RDN_MB 33

A/D_DOCK_PR

CN12

18 USB_PN4_B

L_MDI3+_PR
L_MDI2+_PR
L_TDP_PR
L_RDP_PR

L_MDI3-_PR
L_MDI2-_PR
L_TDN_PR
L_RDN_PR

USB_PP4_B 18

SLCT_STB# 25
LPT_PD1 25
LPT_PD3 25
LPT_PD7 25

PR_IN#_Q

DDC2BD_5 13

25 LPT_PD0
25 LPT_PD2
25 LPT_PD5
25 SLCT_BUSY
13 VSYNC_PB
13 DAC_G_PB

L66 120Ohm/100Mhz

DAC_G_PB_Q

C1095 22PF/25V

+5VS

25 SLCT_PE
25 LPT_PD6
25 SLCT_SLIN#
25 SLCT_ERROR#

SLCT_ACK# 25
LPT_PD4 25
SLCT_INIT# 25
SLCT_AFD# 25
LPT_SLCT 25

+12VS

R824 0Ohm

+5V_PR

13 HSYNC_PB
13 DAC_R_PB

L68 120Ohm/100Mhz

DAC_R_PB_Q

C1097 22PF/25V

C775 0.1UF/25V

DOCKING_68P

DAC_B_PB_Q

DDC2BC_5 13
DAC_B_PB 13

L67 120Ohm/100Mhz

C1096 22PF/25V

12G190006810

R1.1 No32

C1095,C1096,C1097 mount

+5VS

D57 1N4148W

LPT_PD5

R821 2.7KOhm

RP4A

LPT_PD3
LPT_PD7
LPT_PD1
LPT_PD2
LPT_PD4
LPT_PD6
SLCT_SLIN#
SLCT_INIT#

RP5A

SLCT_STB#
SLCT_ERROR#
SLCT_ACK#
SLCT_PE
SLCT_BUSY
LPT_SLCT
SLCT_AFD#
LPT_PD0

2.7KOhm 10 RP4B 10 RP4C 10 RP4D 10 RP4E 10 RP4F 10 RP4G 10 RP4H 10 RP5B 10 RP5C 10 RP5D 10 RP5E 10 RP5F 10 RP5G 10 RP5H

R1.2,No66-4
R1.2 No66-2
R2.0 No71
R2.0 No76
R2.0 No85

20060714 for Napa refresh

OE	S	Out
L	L	B1
L	H	B2
H	X	NC

33 LAN_MDI3-
33 LAN_MDI3+
33 LAN_MDI2-
33 LAN_MDI2+
33 LAN_TDP
33 LAN_TDN
33 LAN_RDP
33 LAN_RDN

LAN_MDI3- R3704 0Ohm L_MDI3-_MB L_MDI3-_PR
LAN_MDI3+ R3701 0Ohm L_MDI3+_MB L_MDI3+_PR
LAN_MDI2- R3702 0Ohm L_MDI2-_PR L_MDI2-_MB
LAN_MDI2+ R3703 0Ohm L_MDI2+_PR L_MDI2+_MB
LAN_TDP L_TDP_MB L_TDP_PR
LAN_TDN L_TDN_MB L_TDN_PR
LAN_RDP L_RDP_PR L_RDP_MB
LAN_RDN L_RDN_PR L_RDN_MB

For Port Bar OC

+5V_PR

+5V

U62 AAT4610AIGV

C776 0.47UF/16V

10KOhm R825

C777 4.7UF/10V

change P/N for buyer:06G030004040

DAC_G_PB
DAC_R_PB
DAC_B_PB

R826 150Ohm
R827 150Ohm
R828 150Ohm

ASUSTek COMPUTER INC. NB6

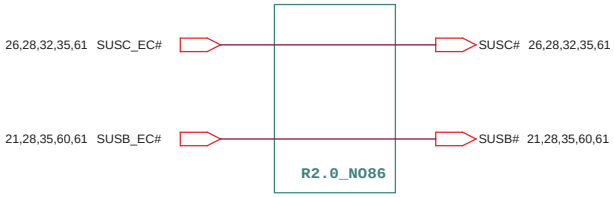
Title : PORT BAR 3 Conn.

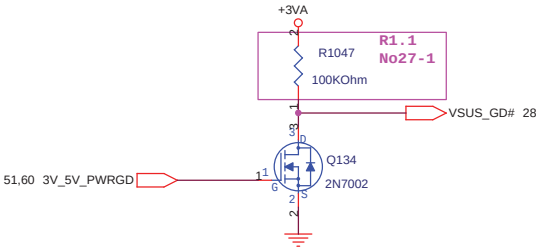
Engineer: Sean1 Chou

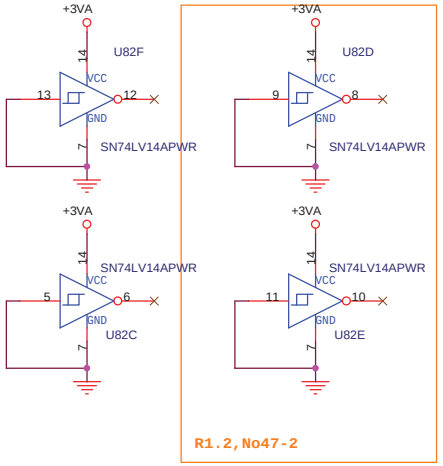
Size	Project Name	Rev
C	Z62J	2.1

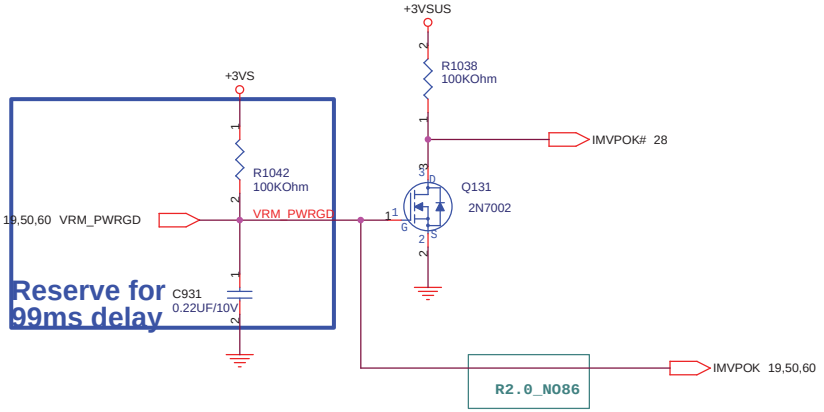
Date: Wednesday, August 16, 2006 Sheet 37 of 69

To Discharge circuits

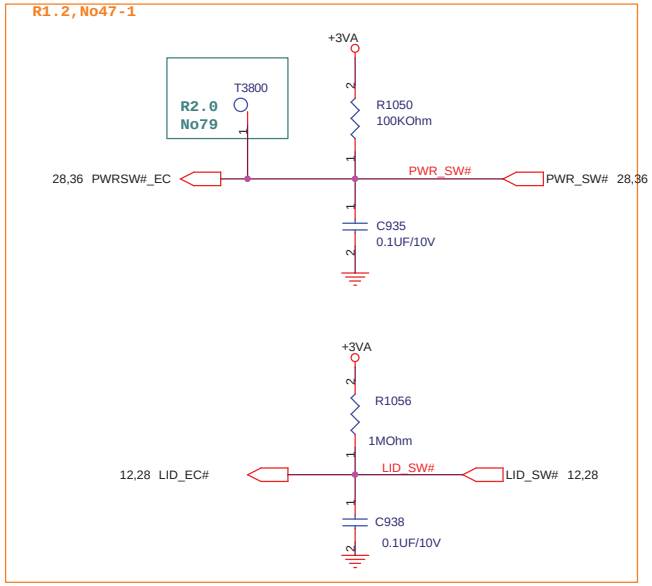






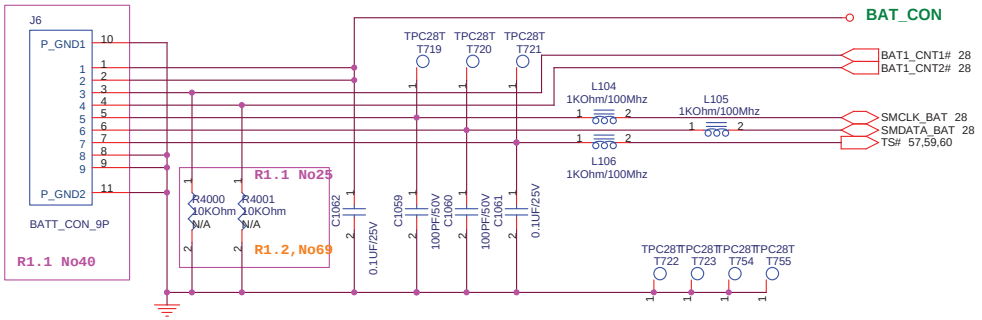


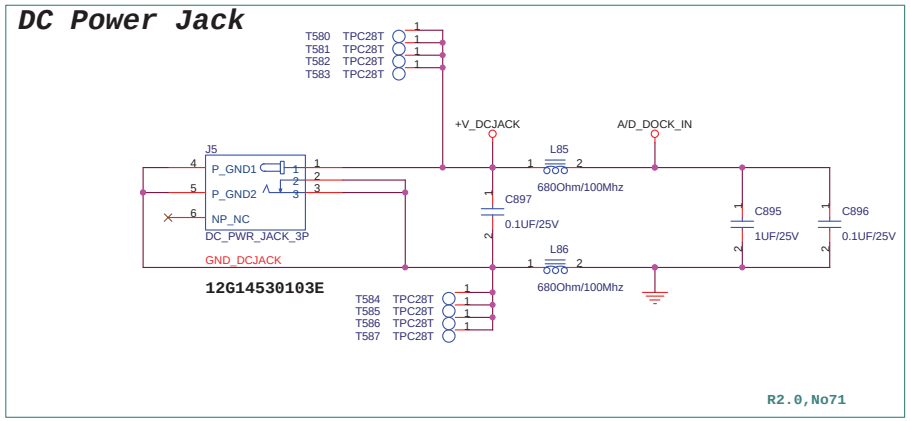
because of LID_SW# and PWR_SW# is connected to EC, we can simplify the circuits.

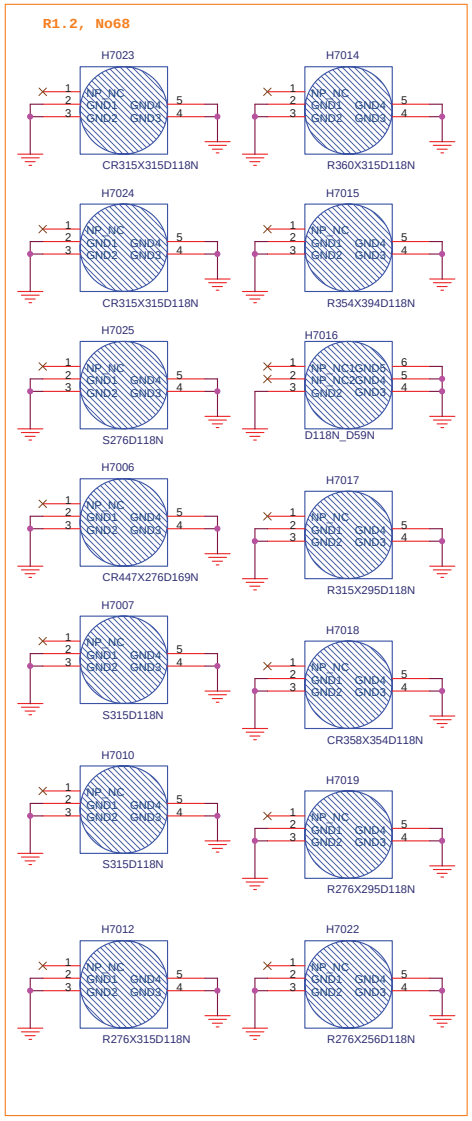


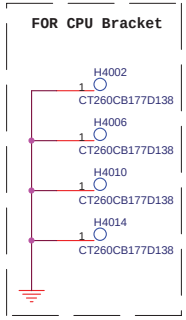
POWER SWITCH

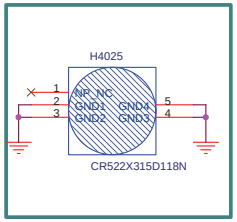
ASUSTek COMPUTER INC. NB6	Title : POWER-ON SEQ.	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 38 of 69	

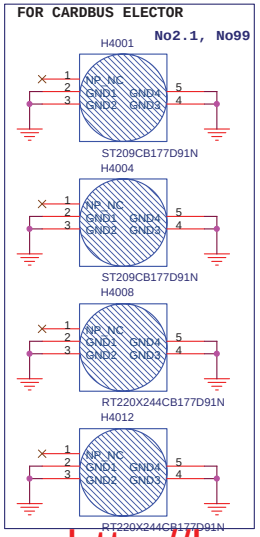


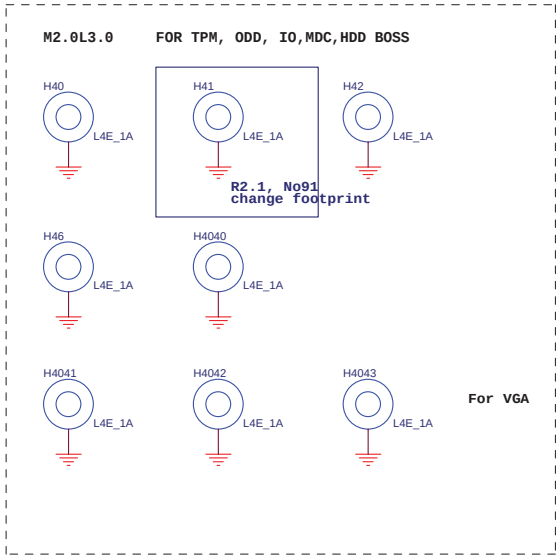


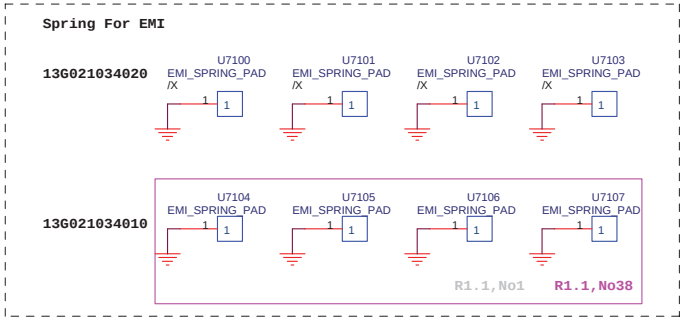












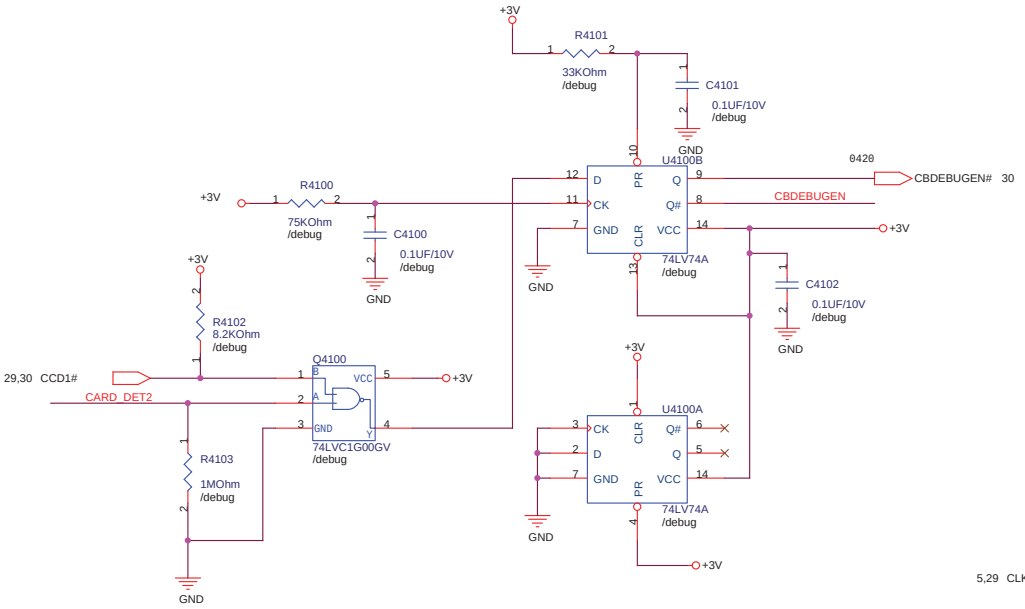
ASUSTek COMPUTER INC. NB6

Title : DC/ BATT IN & Screw Hole

Engineer: Sean1 Chou

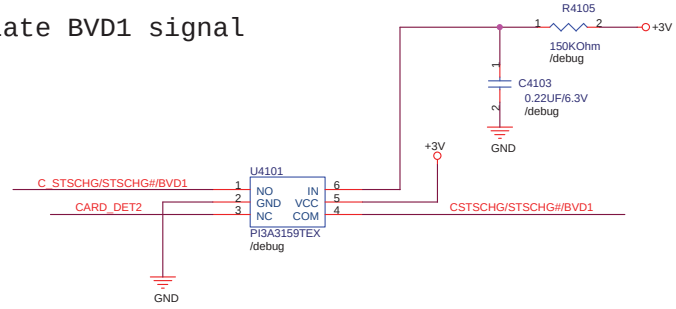
Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 39 of 69



RC value may need to tuned for each product.

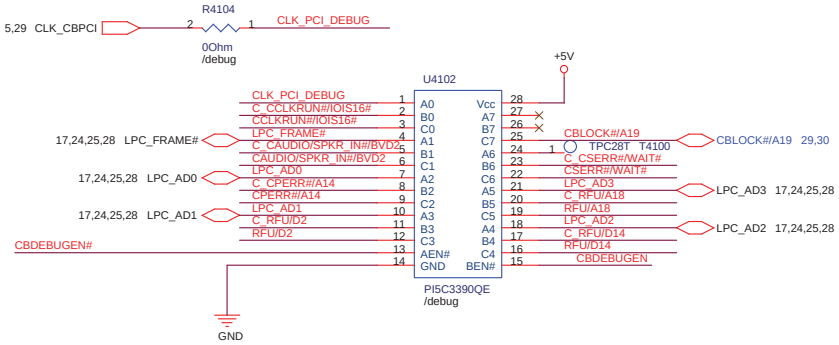
Isolate BVD1 signal

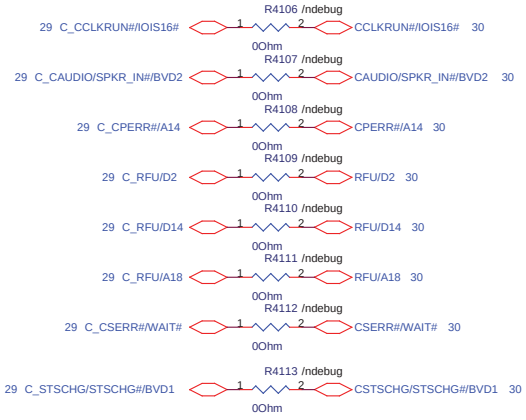


When +3V on, select BVD1 to CARD_DET2 for RC delay time

PCMCIA DEBUG PORT

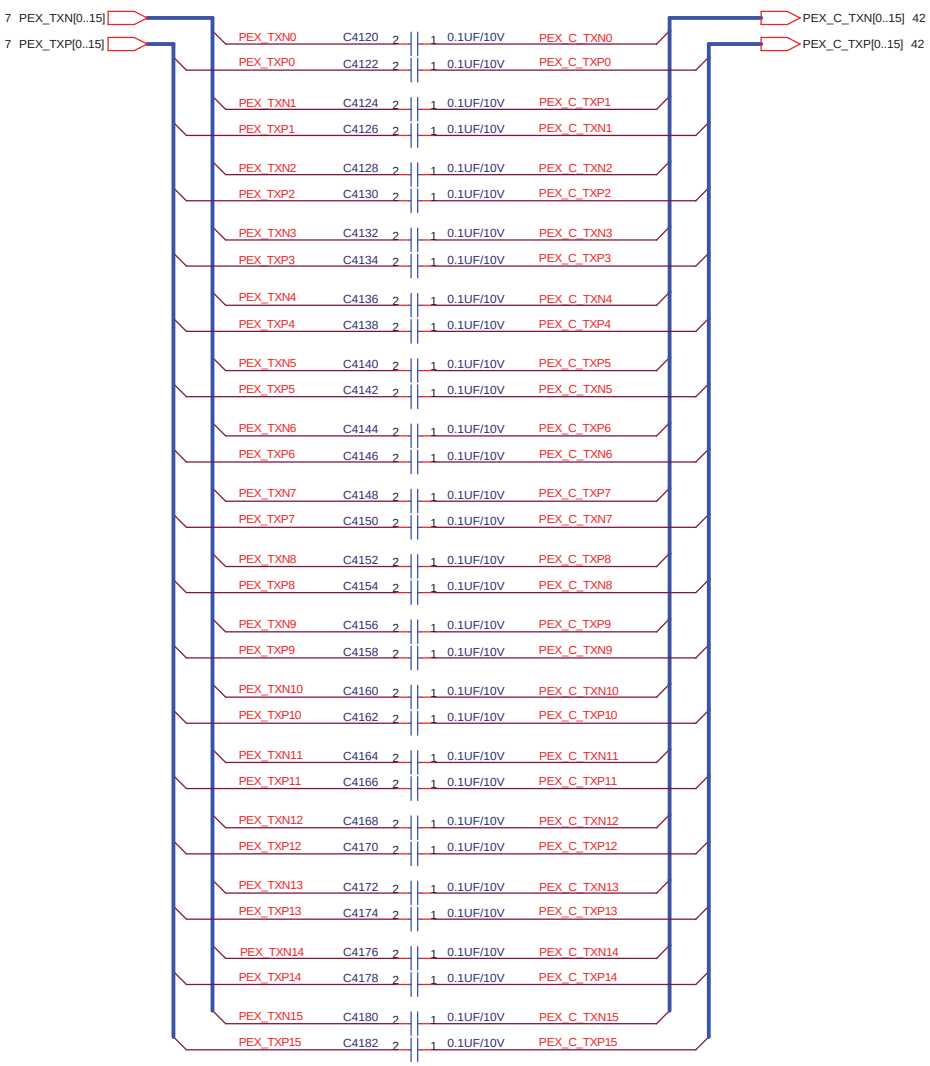
Isolate card bus control and slot signal when debug card plug in





Title : PCMCIA Debug		
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 40 of 69	

PEX_C_TXN1,5,6,7,8,9 polarity reverse



PLACE these 0402 AC coupling caps close to 945PM.

PEX_RXN13 polarity reverse

PLACE these 0402 AC coupling caps close to G72M

ASUSTek COMPUTER INC. NB6

Title : PCIE AC COUPLE

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

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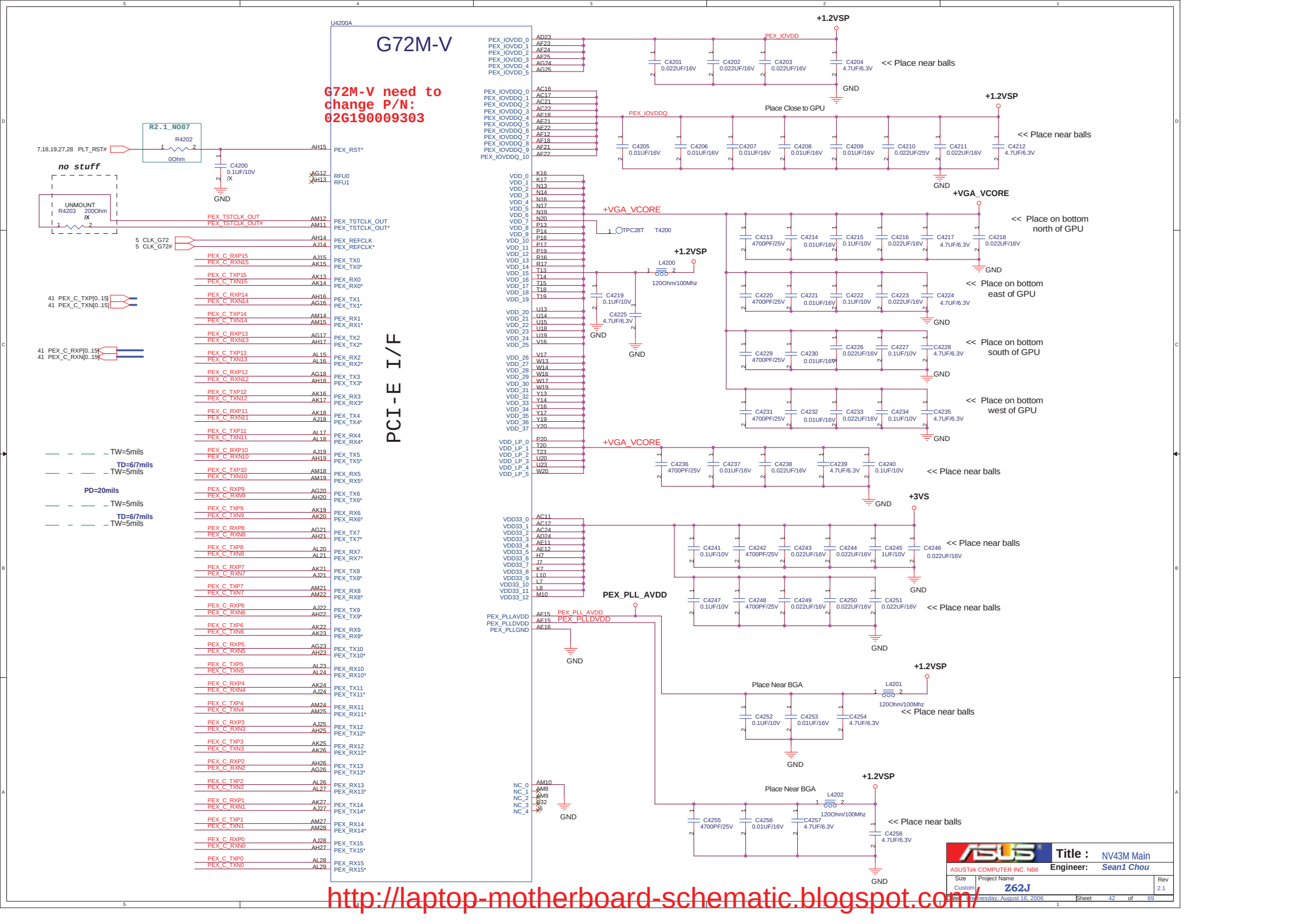


FOR MEMORY STRAPS

U4200E

G72M-V

STRAP (F1) — NC FOR NV44

MEMSTRAPSEL0 (AE26), MEMSTRAPSEL1 (AD26), MEMSTRAPSEL2 (AH31), MEMSTRAPSEL3 (AH32)

RFU6 (U3), RFU7 (V3), RFU8 (U6), RFU9 (U5), RFU10 (U4), RFU11 (V4), RFU12 (V6)

ROMCS* — AA4 NVROMCS — TPC28T T4300

ROM_SO — AA6 — TPC28T T4301

ROM_SI — W2 — TPC28T T4302

ROM_SCLK — AA7 — TPC28T T4303

I2CH_SCL — G3 HDCPROMSCL — TPC28T T4304

I2CH_SDA — H3 HDCPROMSDA — TPC28T T4305

BUFRST* — F3 — TPC28T T4306

STEREO — T3 — TPC28T T4307

SWAPRDY_A — M6 SWAPRDY_A — TPC28T T4308

TESTMEMCLK — A26 TESTMEMCLK — R4300 2 — 1 10KOhm

TESTMODE — H2 TESTMODE — R4305 2 — 1 10KOhm

MCG0 — AL10

MCG1 — AG13

GND

FOR MEMORY STRAPS

U4200K

G72M-V

+3VS — C4300 0.1UF/10V — PLACE CAPS & RES CLOSE TO GPU PINS

MIOA_VDDQ_0 (M7), MIOA_VDDQ_1 (M8), MIOA_VDDQ_2 (R8), MIOA_VDDQ_3 (T8), MIOA_VDDQ_4 (U9)

MIOACAL_PD_VDDQ — TPC28T T4309 — L1

MIOACAL_PU_GND — TPC28T T4310 — L3

MIOA_VREF — L2

+3VS — R4315 1KOhm /X — MIOA_VREF — R4317 1KOhm /X — C4301 0.1UF/10V /X — GND

MIOAD0 (P2), MIOAD1 (N2), MIOAD2 (N1), MIOAD3 (N3), MIOAD4 (M1), MIOAD5 (M3), MIOAD6 (P5), MIOAD7 (N6), MIOAD8 (N5), MIOAD9 (M4), MIOAD10 (L4), MIOAD11 (L5)

MIOAD0 — MIOAD1 — MIOAD2 /X — MIOAD3 /X — MIOAD4 /X — MIOAD5 /X — MIOAD6 — MIOAD8 — MIOAD9

+3VS — R4328 10KOhm /X — R4329 10KOhm /X — R4330 10KOhm /X — R4331 10KOhm /X

MIOAD7 : TVMODE0

MIOAD10 : TVMODE1

MIOA_HSYNC : GPU MCH share ref clk or not

MIOA_HSYNC (R3), MIOA_VSYNC (R1), MIOA_DE (P1), MIOA_CTL3 (P3) — R4316 2KOhm /X — GND

MIOA_CLKOUT (R4), MIOA_CLKOUT* (P4), MIOA_CLKIN (M5) — R4318 10KOhm /X — GND

check: need mount or not

MIOAD1 — R4314 2KOhm — For System BIOS

STRAP= 0: System BIOS

STRAP= 1: Adapter BIOS

GND

FOR CRYSTAL / PCIE_ID STRAPS

U4200N

G72M-V

+3VS — C4302 0.1UF/10V — PLACE CAPS CLOSE TO GPU PINS

MIOB_VDDQ_0 (AA8), MIOB_VDDQ_1 (AB7), MIOB_VDDQ_2 (AB8), MIOB_VDDQ_3 (AC6), MIOB_VDDQ_4 (AC7)

MIOBCAL_PD_VDDQ — TPC28T T4313 — Y1

MIOBCAL_PU_GND — TPC28T T4314 — Y3

MIOB_VREF — Y2

+3VS — R4323 1KOhm /X — MIOB_VREF — R4326 1KOhm /X — C4303 0.1UF/10V /X — GND

MIOBD0 (AC3), MIOBD1 (AC1), MIOBD2 (AC2), MIOBD3 (AB2), MIOBD4 (AB1), MIOBD5 (AA1), MIOBD6 (AB3), MIOBD7 (AA3), MIOBD8 (AC5), MIOBD9 (AB5), MIOBD10 (AB4), MIOBD11 (AA5), RFU13 (W3), RFU14 (V1), RFU15 (Y5), RFU16 (W1), RFU17 (W4), RFU18 (W5), RFU19 (V5), RFU20 (Y6)

MIOBD0 — MIOBD1 — VIPD2 — TPC28T T4311 — VIPD3 — VIPD4 — VIPD5 — VIPD6 — VIPD7 — TPC28T T4312 — MIOBD8 — MIOBD9 — MIOBD11

+3VS — R4319 2KOhm /X — R4322 2KOhm — GND

MIOBD10 : ROMTYPE0

MIOB_VSYNC (AE3), MIOB_HSYNC (AE3), MIOB_DE (AD1), MIOB_CTL3 (AD3)

MIOB_VSYNC : ROMTYPE1

MIOB_CLKOUT (AD4), MIOB_CLKOUT* (AD5), MIOB_CLKIN (AE4) — R4327 10KOhm /X — GND

3GIO PADCFG STRP

02 (0010) NV43/44M

04 (0100) G72

+3VS — R4301 2KOhm /X — MIOAD0

+3VS — R4302 2KOhm — MIOAD6

R1.1, No3

+3VS — R4308 2KOhm /X — MIOAD8

+3VS — R4309 2KOhm /X — MIOAD9

MEM TYPE STRAP

R1.1, No34

G72:

RAM_CFG[3:0] Config FB Bus Width Definitions

0000 16Mx16 DDR2 64-bit Elpida

0001 16Mx16 DDR2 64-bit Samsung

0010 16Mx16 DDR2 64-bit Infineon

0011 16Mx16 DDR2 64-bit Hynix

0100 64-bit Reserved

0101 32Mx16 DDR2 64-bit Samsung

0110 32Mx16 DDR2 64-bit Infineon

0111 32Mx16 DDR2 64-bit Hynix

Samsung needs: --> unmount R4304, R4307, mount R4306, R4303

MIOBD0 : RAMCFG0 MIOBD1 : RAMCFG1

MIOBD8 : RAMCFG2 MIOBD9 : RAMCFG3

+3VS — R4303 10KOhm N/A — MIOBD0 — GND

+3VS — R4304 10KOhm /X — MIOBD1 — GND

+3VS — R4307 10KOhm /X — GND

+3VS — R4306 10KOhm N/A — GND

+3VS — R4310 10KOhm /X — MIOBD8 — R4312 10KOhm — GND

+3VS — R4311 10KOhm /X — MIOBD9 — R4313 10KOhm — GND

(for panel user ID)

MIOAD[2:5] : USER[0:3]

(PCI_DEVICE_ID)

MIOBD4 : PCI_DEVID0 MIOBD3 : PCI_DEVID2

MIOBD5 : PCI_DEVID1 MIOBD11 : PCI_DEVID3

NV43M - ID 0X0168

NV43M-V- ID 0X0167

+3VS — R4320 2KOhm — VIPD4

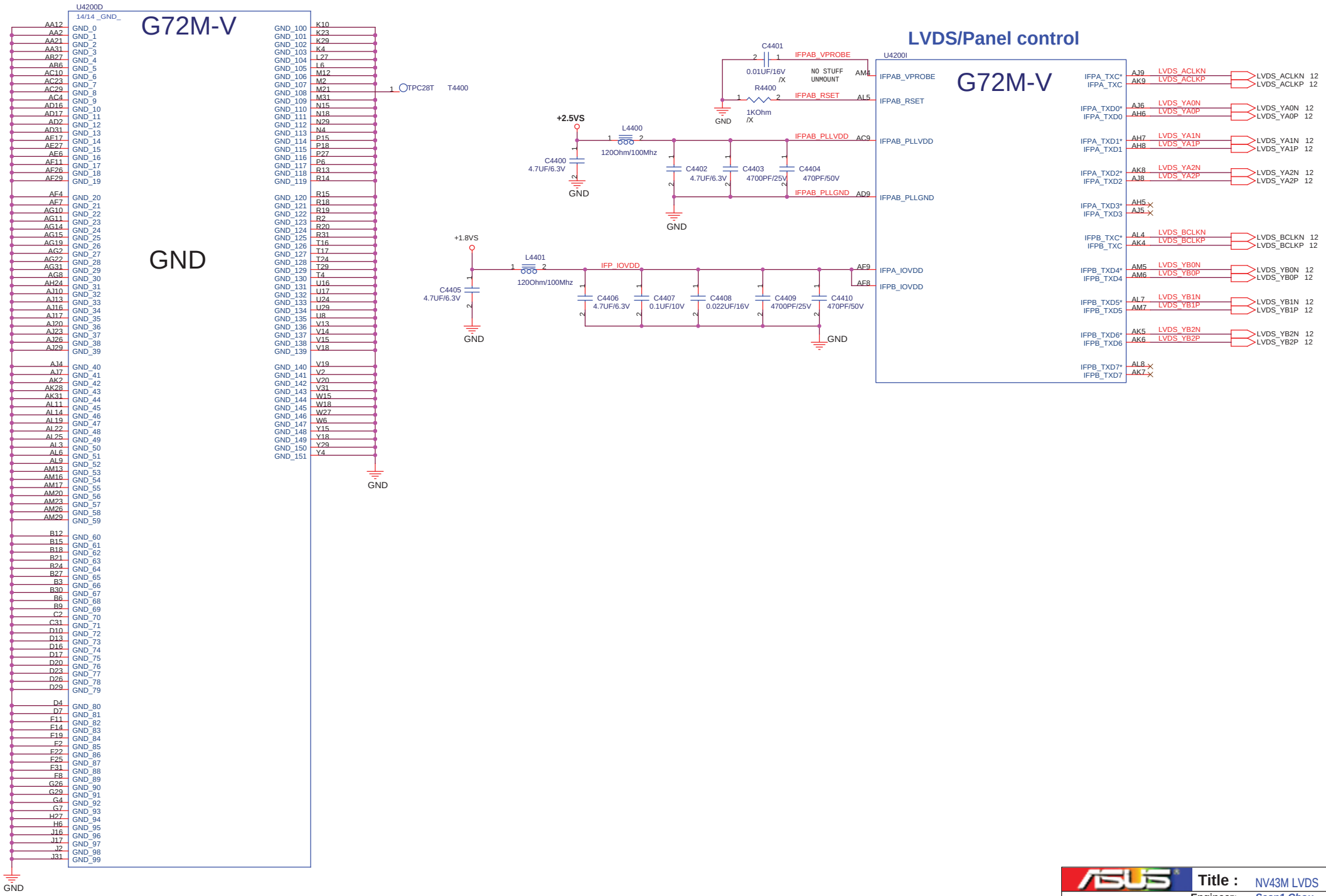
+3VS — R4321 2KOhm — VIPD3

+3VS — R4324 2KOhm — VIPD5

+3VS — R4325 2KOhm /X — MIOBD11

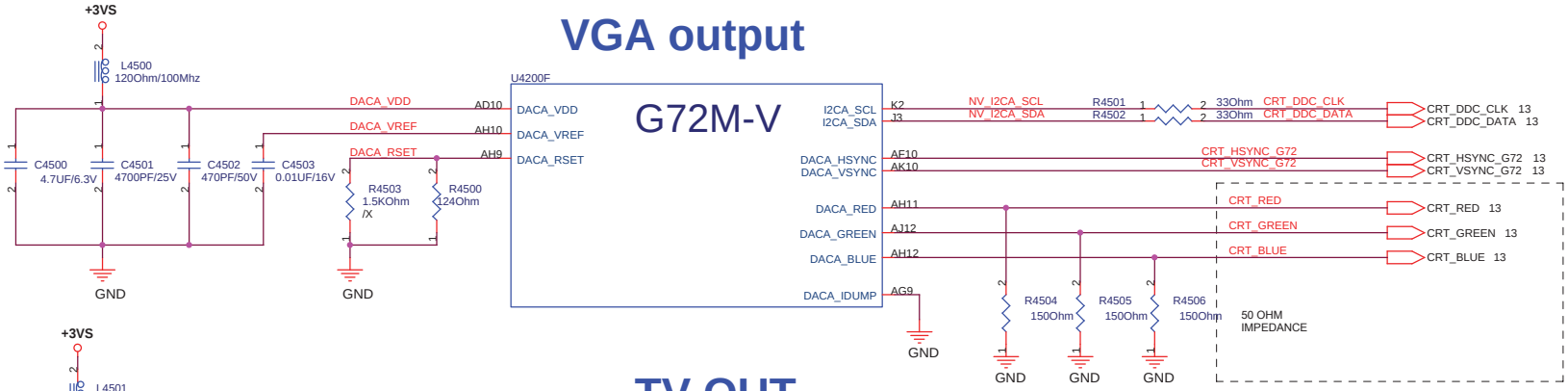
no stuff UNMOUNT

Title :	NV43 Strapping
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou
Size: Custom	Project Name: Z62J
Rev: 2.1	
Date: Wednesday, August 16, 2006	Sheet 43 of 69

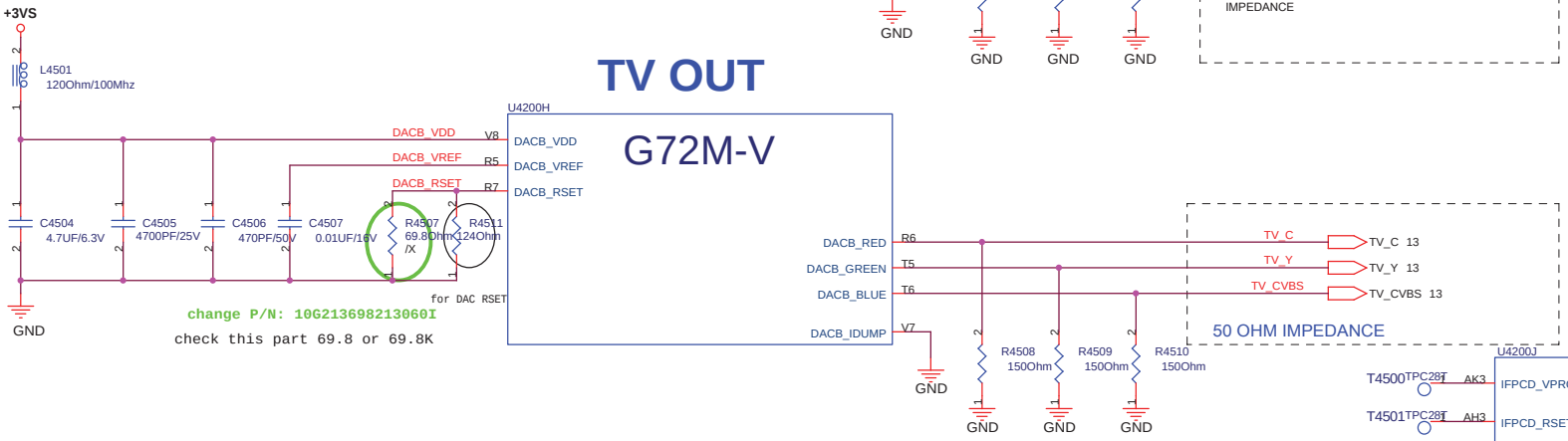


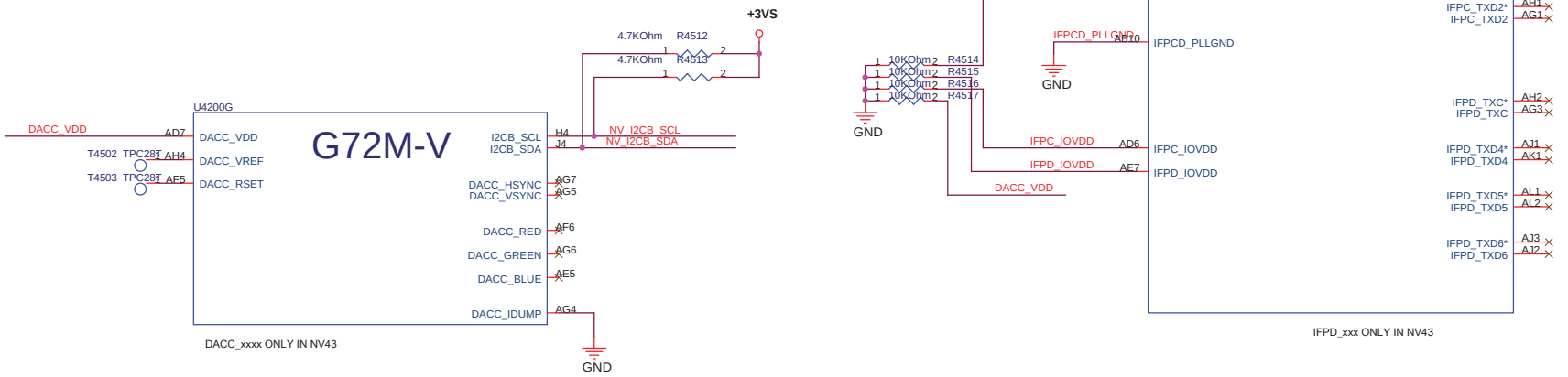
Title :	NV43M LVDS	
ASUSTek COMPUTER INC. NB6	Engineer:	Sean1 Chou
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 44 of 69	

VGA output



TV OUT





<variant_name>

ASUSTek COMPUTER INC. NB6	Title : MV43 VGA/TV Out	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 45 of 69	

XTAL/PLLVDD

PLLVDD-- 3.3V +/- 5% Imax= 25mA

DISP_PLLVDD-- 3.3V +/- 5% Imax=30mA

XTALIN is 1.2V tolerant
3.2V * 150 / (33+270+150) = 1.06

The following must be verified:
MIN Rise Time at XTALIN = 0.133 V/ns
using 10% - 90% with Vmax = 1.3V and
Vmin = -0.7V

R1.1 No35

R1.1 No33
R1.2, No58
R2.1, No88

Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

R1.1 No29-2

check: leakage current

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOT PLUG
1	IN	N/A	2ND DVI HOT PLUG
2	OUT	HIGH	BACKLIGHT BRIGHTNESS
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID0
6	OUT	HIGH	NVVDD VID1
7	OUT	HIGH	FBVDD VID0
8	IN	LOW	THERMAL SHUTDOWN
9	OUT	LOW	THERM ALERT

GPIO & JTAG

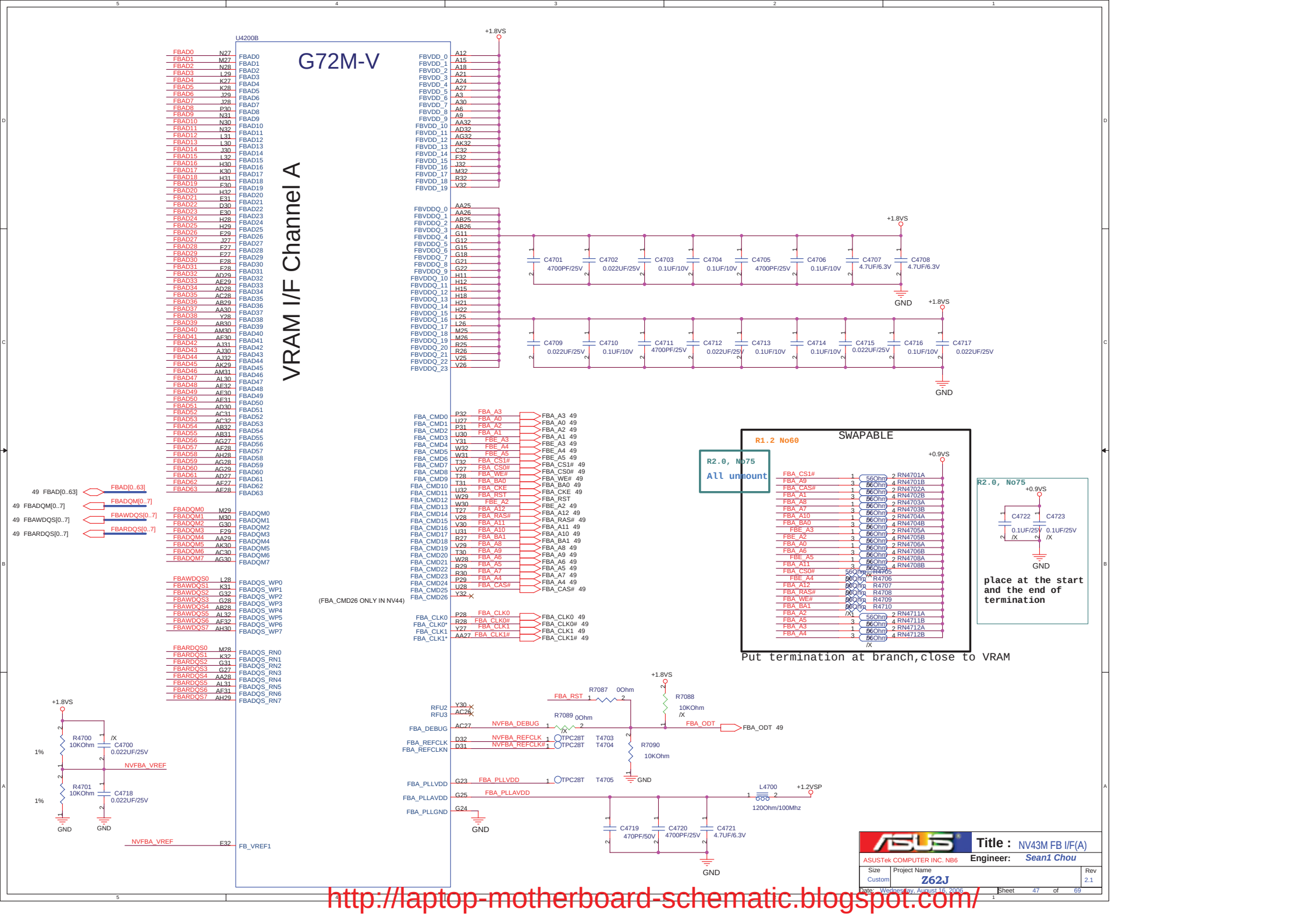
R2.0 No84

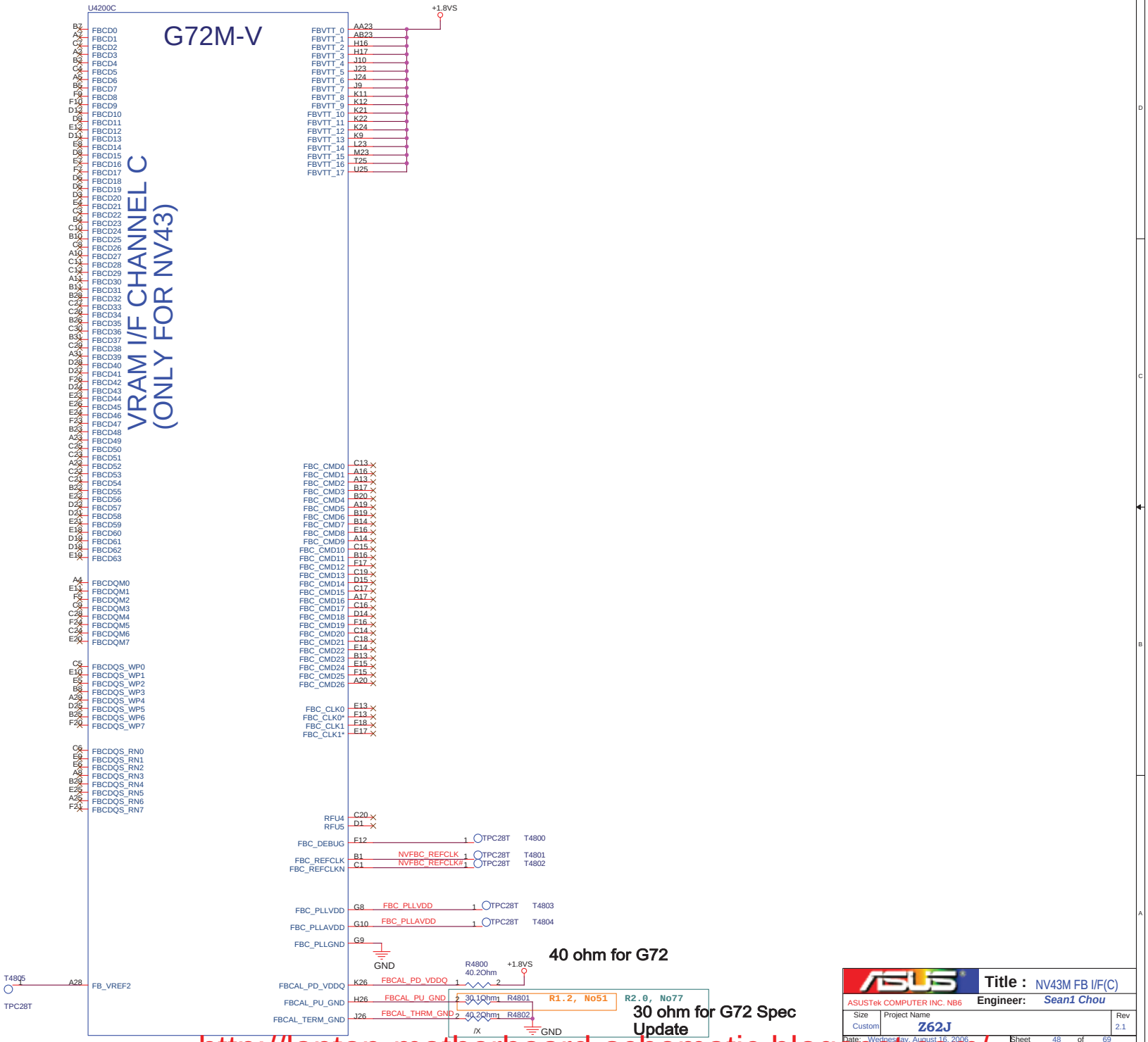
Title : NV Spread Spectrum

ASUSTek COMPUTER INC. NB6 Engineer: Sean1 Chou

Size: Custom | Project Name: Z62J | Rev: 2.1

Date: Wednesday, August 16, 2006 | Sheet 46 of 69


G72M-V
VRAM I/F Channel A
U4200B
SWAPABLE
R1.2 No60
R2.0, No75
All unmount
R2.0, No75
place at the start and the end of termination
Put termination at branch,close to VRAM
(FBA_CMD26 ONLY IN NV44)
Title : NV43M FB I/F(A)
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 47 of 69
http://laptop-motherboard-schematic.blogspot.com/



R1.2 No65

DDR2/16M*16-2.5 1.8V

03G151236011	INFINEON/HYB18T256161AFL-25
03G151236114	SAMSUNG/K4N56163QG-ZC25
03G151236210	HYNIX/HY5PS561621AFP-25

Swapable

Swapable

R1.1 R19

VRAM change P/N:
03G151236114

U4900 / U4901 / U4902 / U4903 — K4N56163QF-ZC25

Place near U4901

Place near U4903

VDD/VDDQ = 1.8V

Place near right VRAM >>

<< Place near left VRAM

VREF=0.4(FBVDDQ) FOR NV44

VREF=0.4(FBVDDQ) FOR NV44

FBA_ODT 47

FBAD[0..63] 47

FBADQM[0..7] 47

FBAWDQS[0..7] 47

FBARDQS[0..7] 47

FBA_A3 47
FBA_A0 47
FBA_A2 47
FBA_A1 47
FBE_A3 47
FBE_A4 47
FBE_A5 47
FBA_CS1# 47
FBA_CS0# 47
FBA_WE# 47
FBA_BA0 47
FBA_CKE 47
FBA_RST 47
FBE_A2 47
FBA_A12 47
FBA_RAS# 47
FBA_A11 47
FBA_A10 47
FBA_BA1 47
FBA_A8 47
FBA_A9 47
FBA_A6 47
FBA_A5 47
FBA_A7 47
FBA_A4 47
FBA_CAS# 47

FBA_CLK0 47
FBA_CLK0# 47
FBA_CLK1 47
FBA_CLK1# 47

Title : NV43M VRAM(A)

ASUSTek COMPUTER INC. NB6

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

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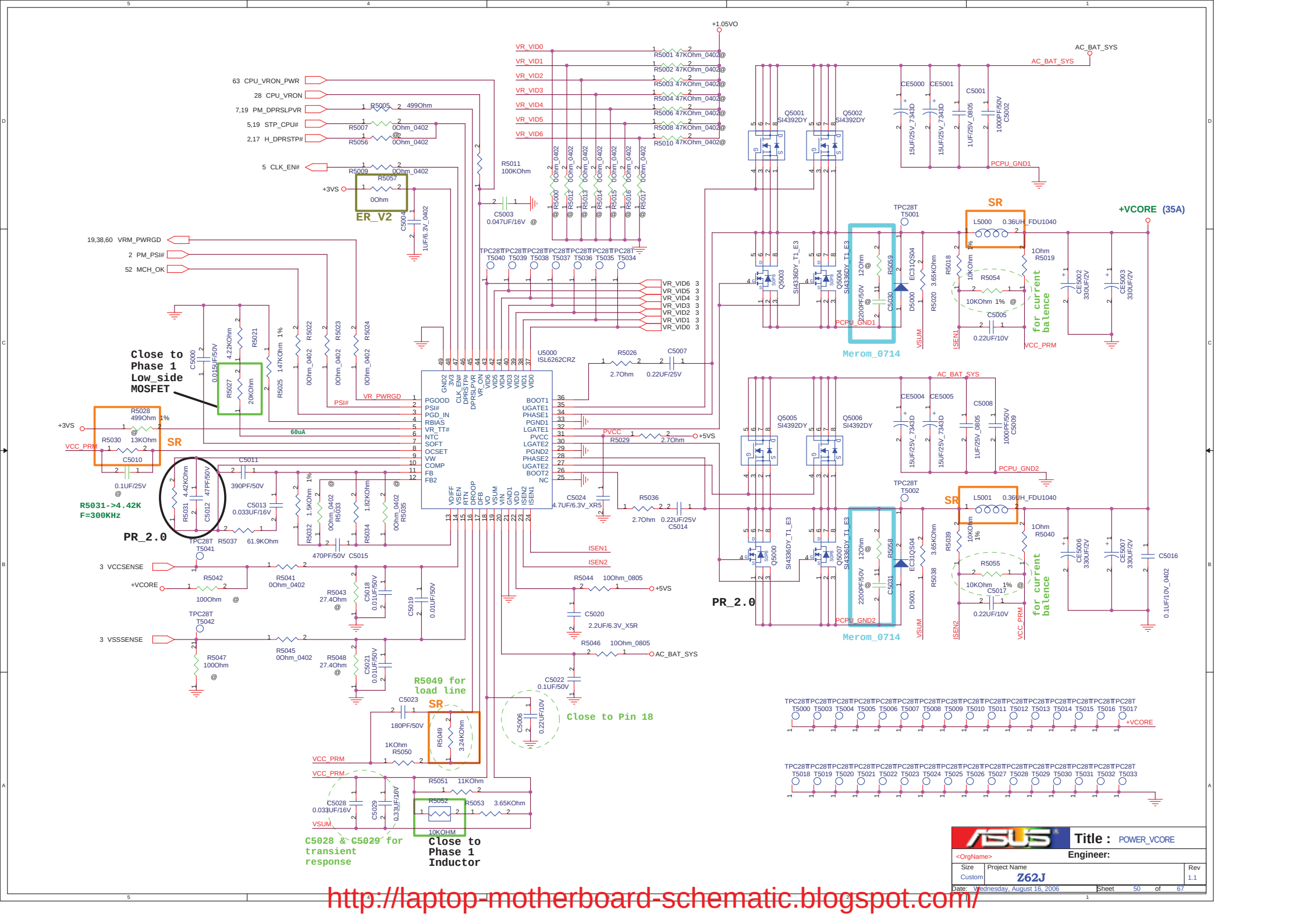
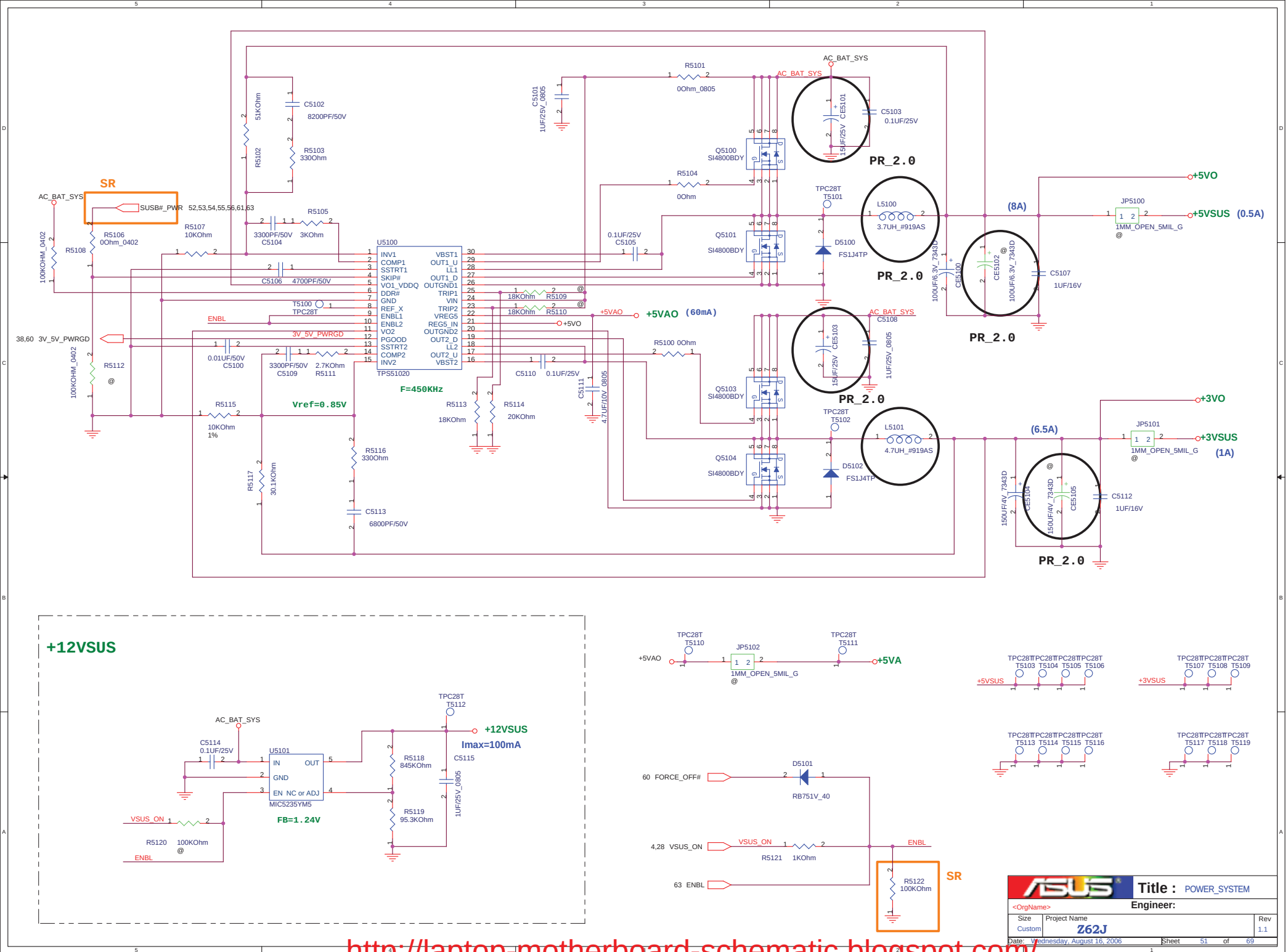
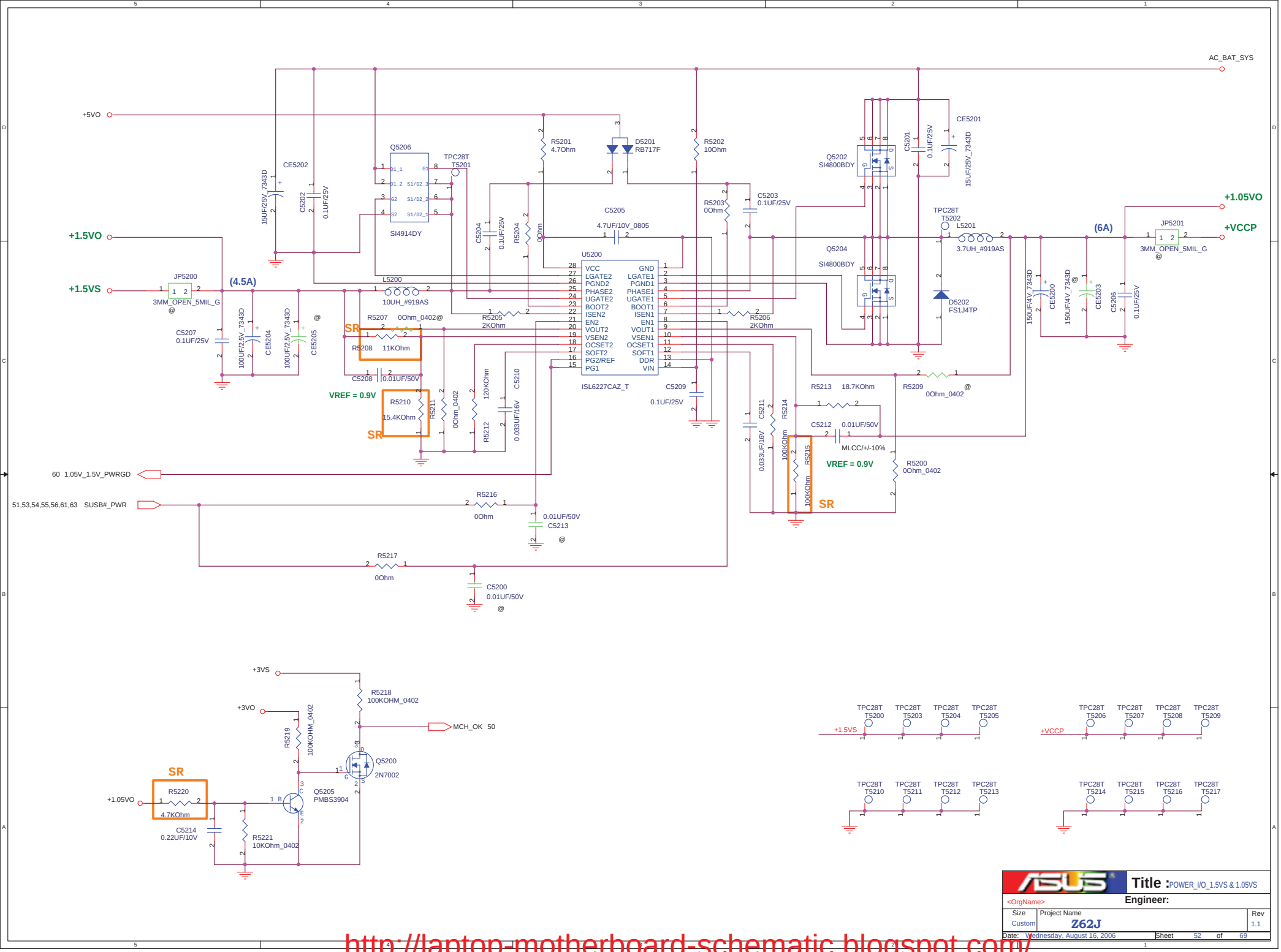
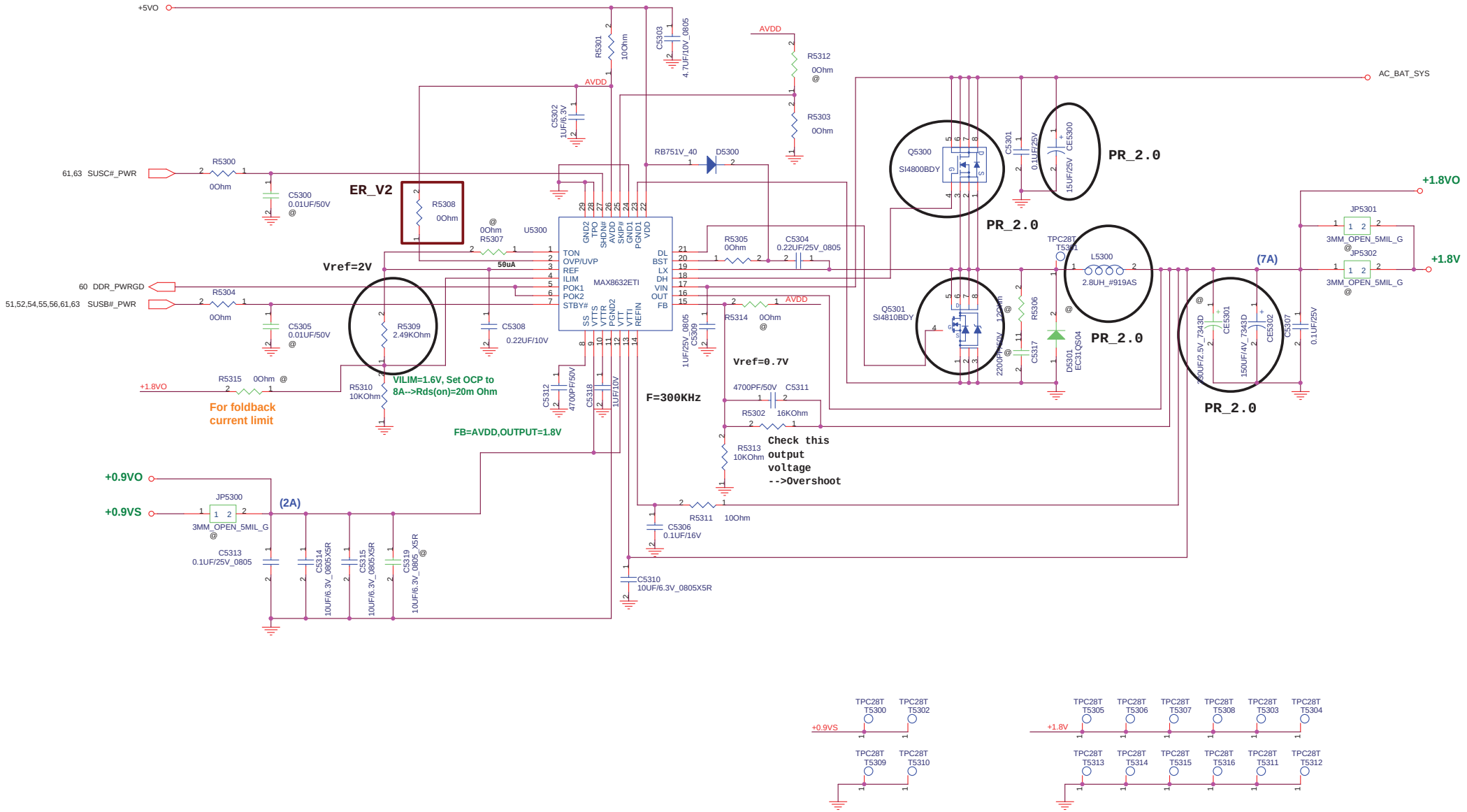


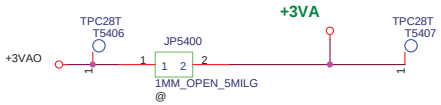


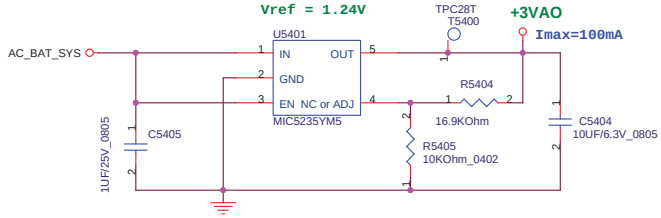




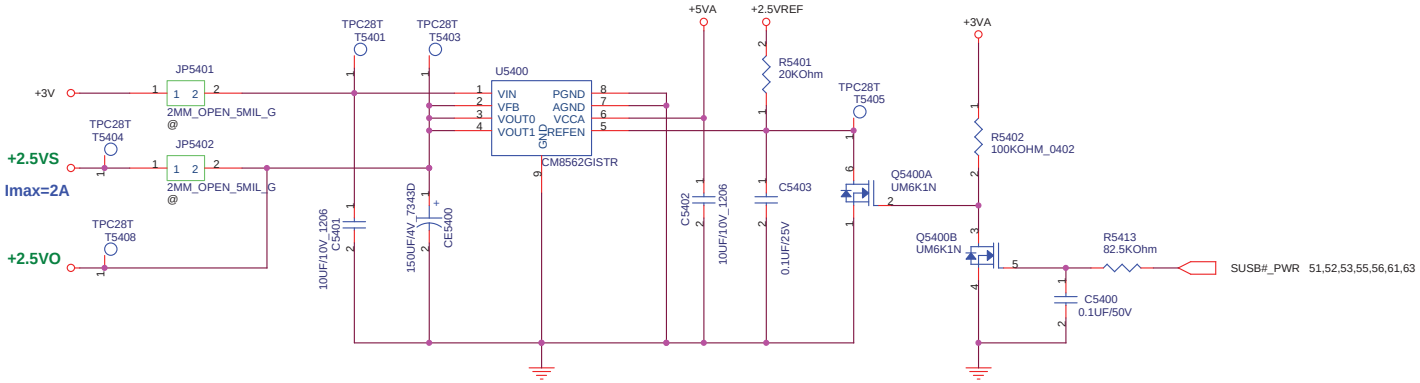
Title :	POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 53 of 69	

+3VA0

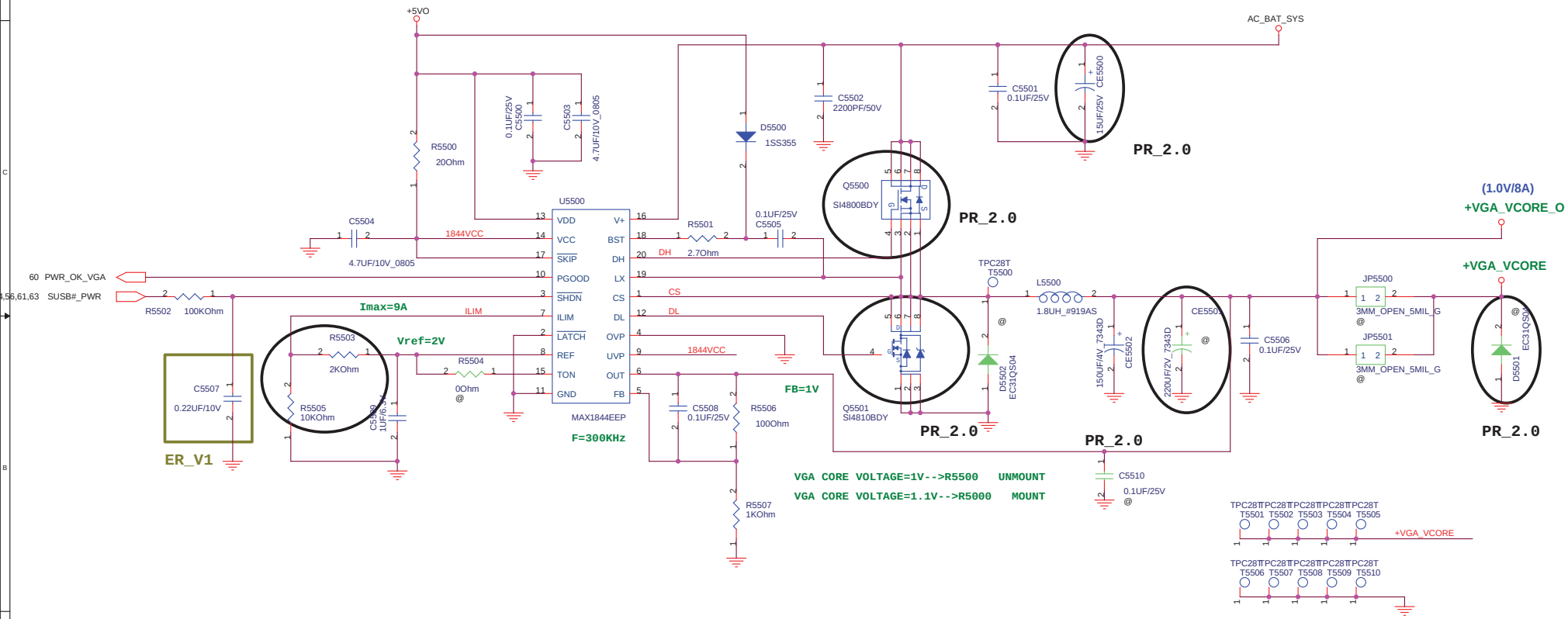




+2.5VS

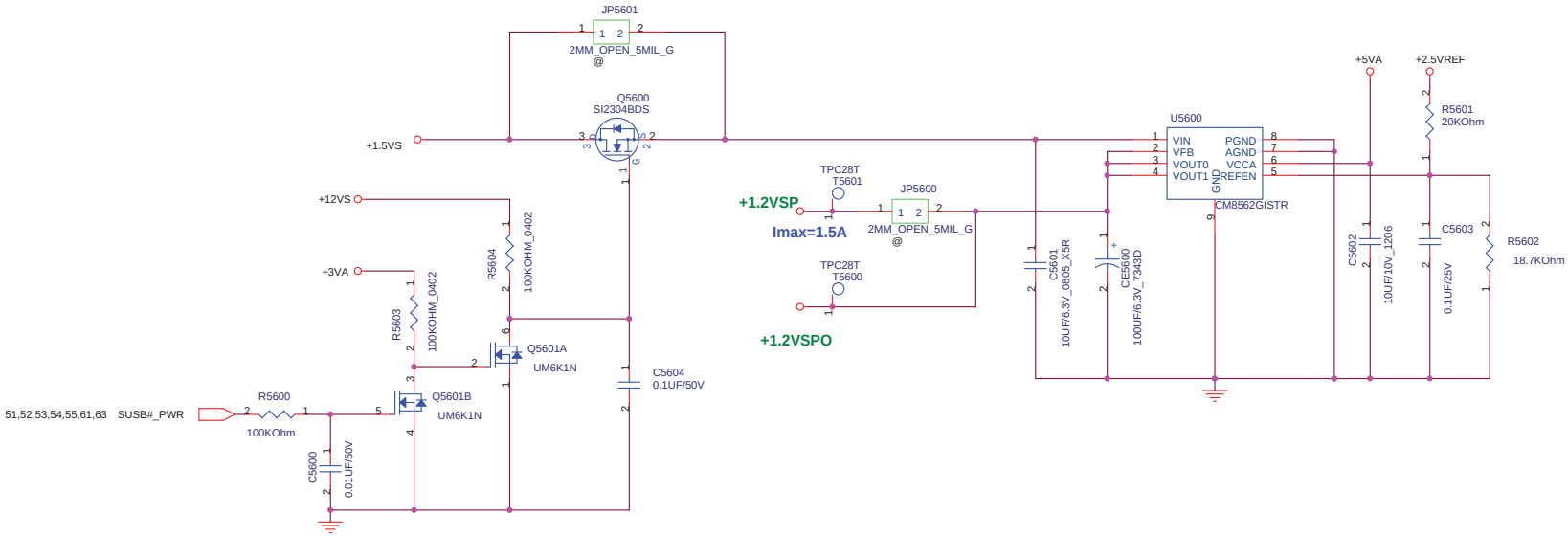


ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 54 of 69	

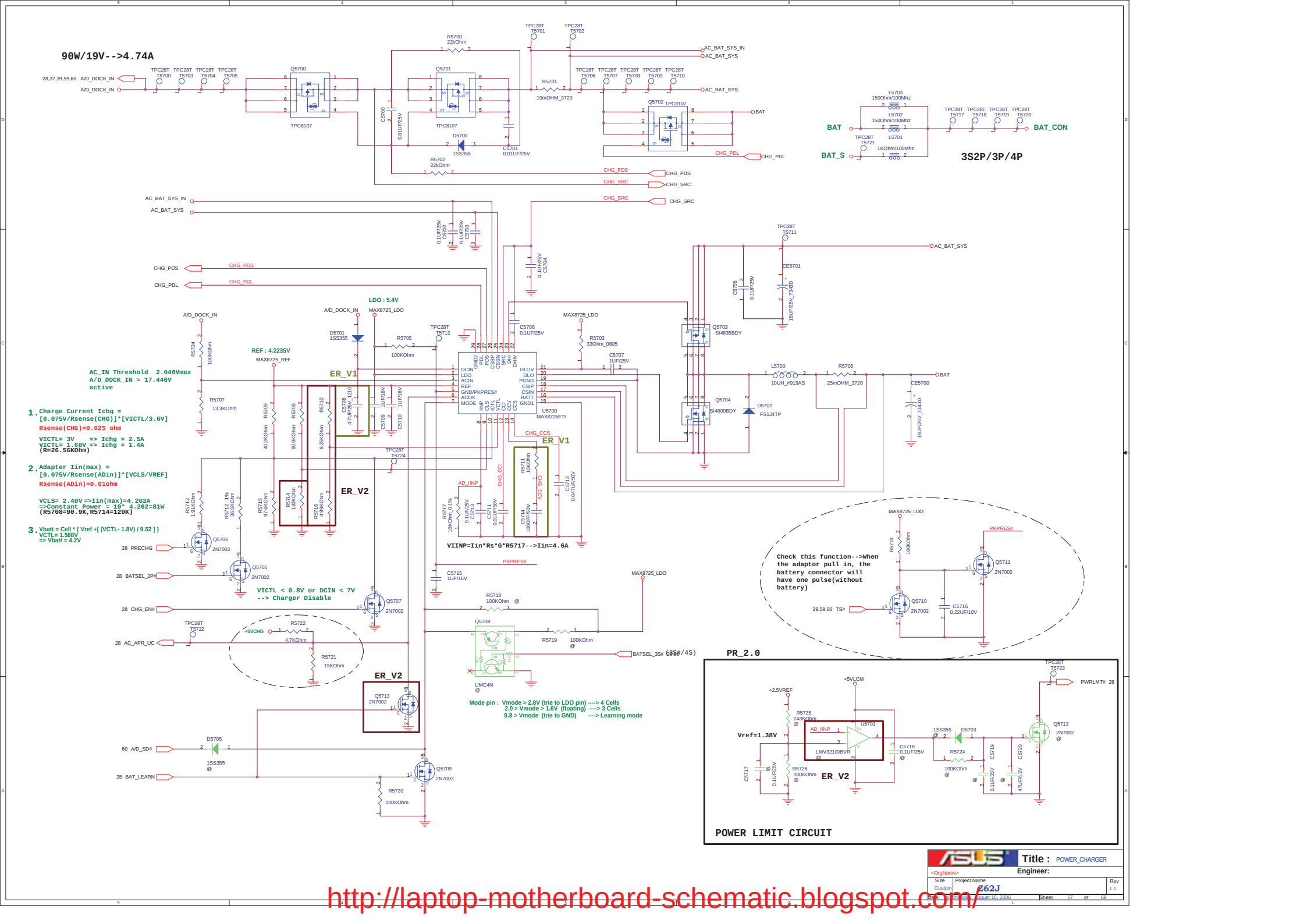


ASUS	Title : POWER_VGA_CORE		
<OrgName>	Engineer:		
Size: Custom	Project Name: Z62J		Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 55 of 69		

+1.2VSP

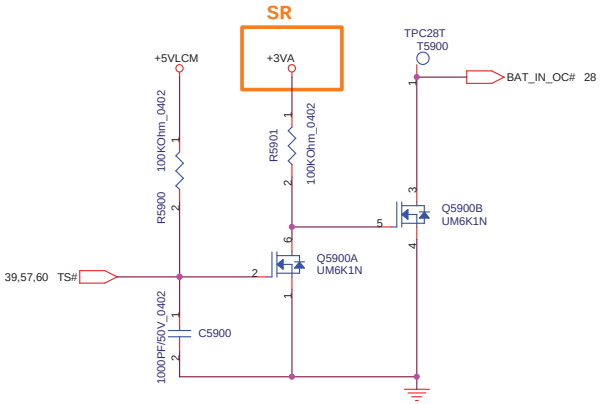


ASUS	Title : POWER_+1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 56 of 69	

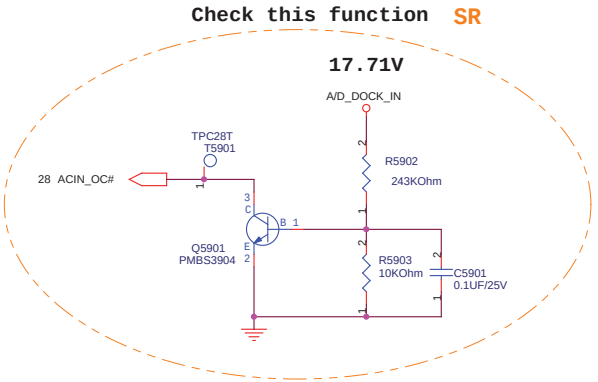


Title :	POWER_PIC			
<OrgName>	Engineer:			
Size: Custom	Project Name: Z62J			Rev: 1.1
Date: Wednesday, August 16, 2006		Sheet 58 of 69		

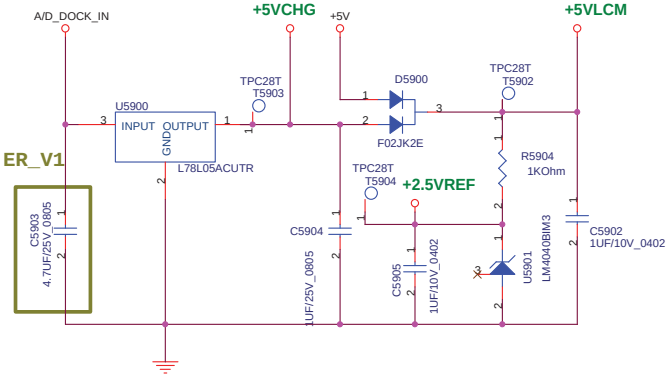
BATTERY IN DETECT



ADAPTER IN DETECT

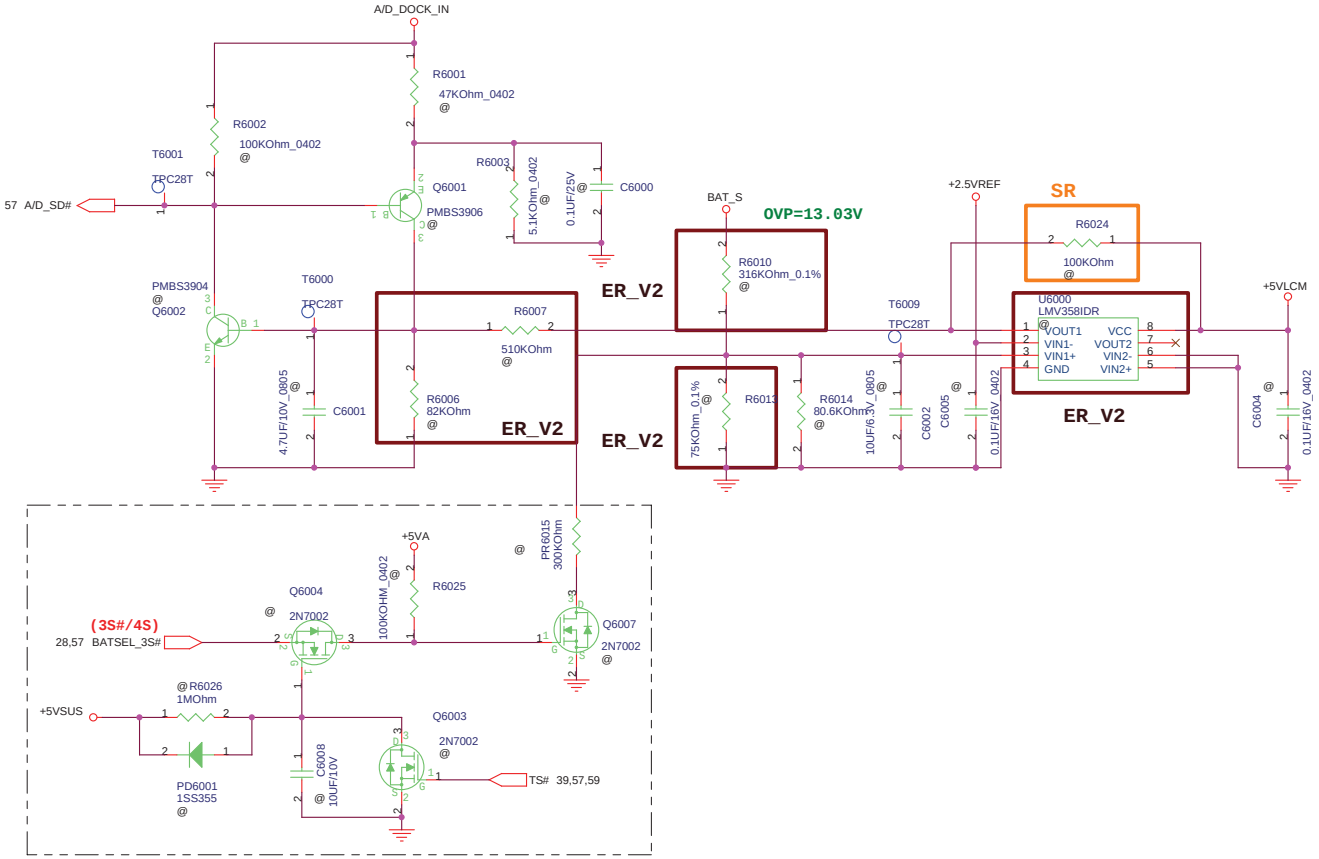


+5VLCM, +5VCHG & +2.5VREF

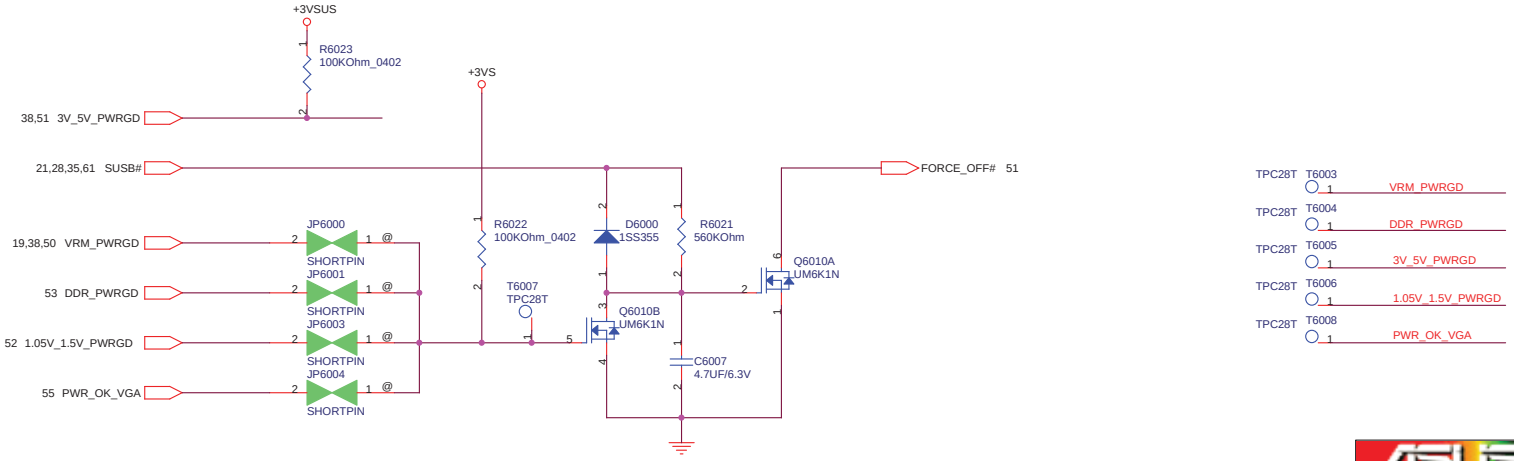


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 59 of 69	

BATTERY A/D_SD# (OVP)

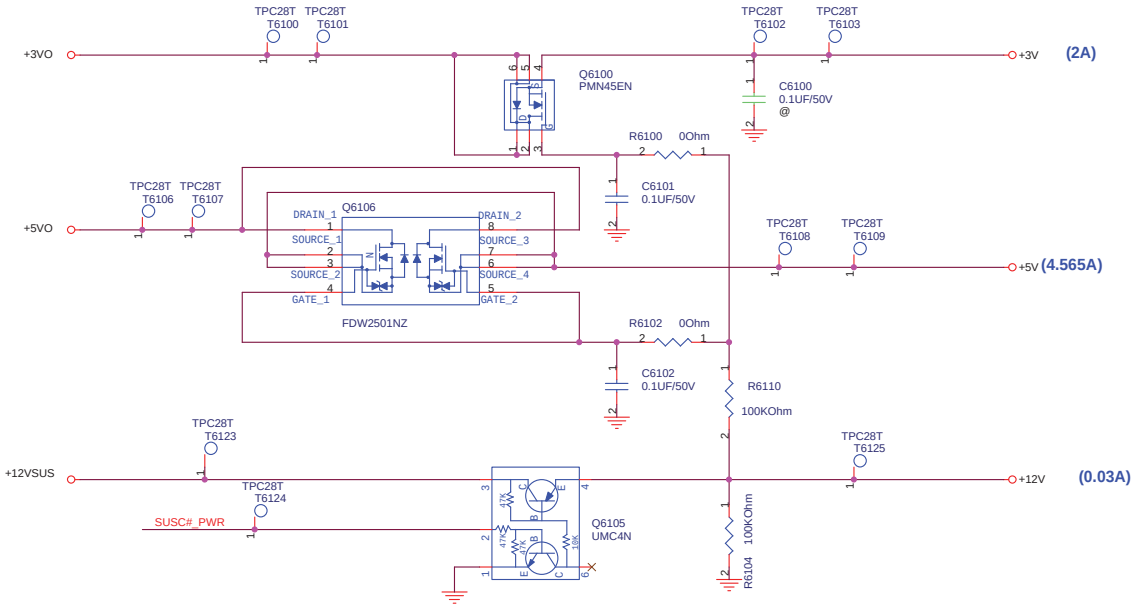


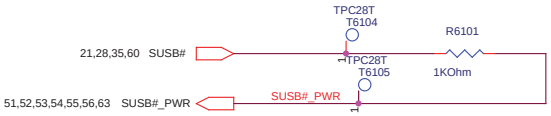
POWER GOOD DETECTER



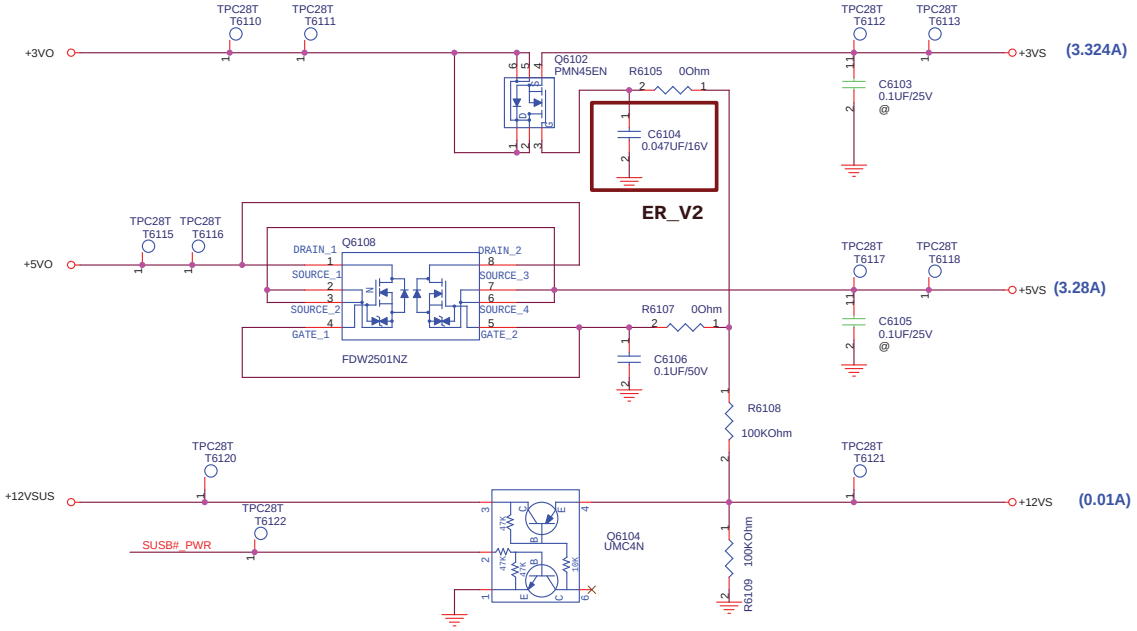
ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 60 of 69	

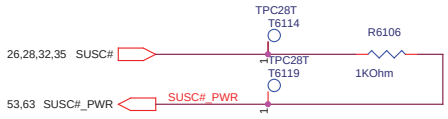
SUSC#_PWR POWER

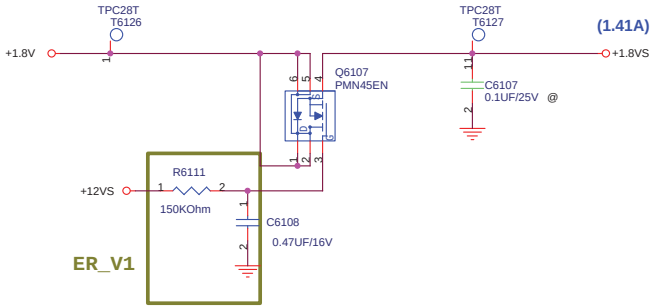




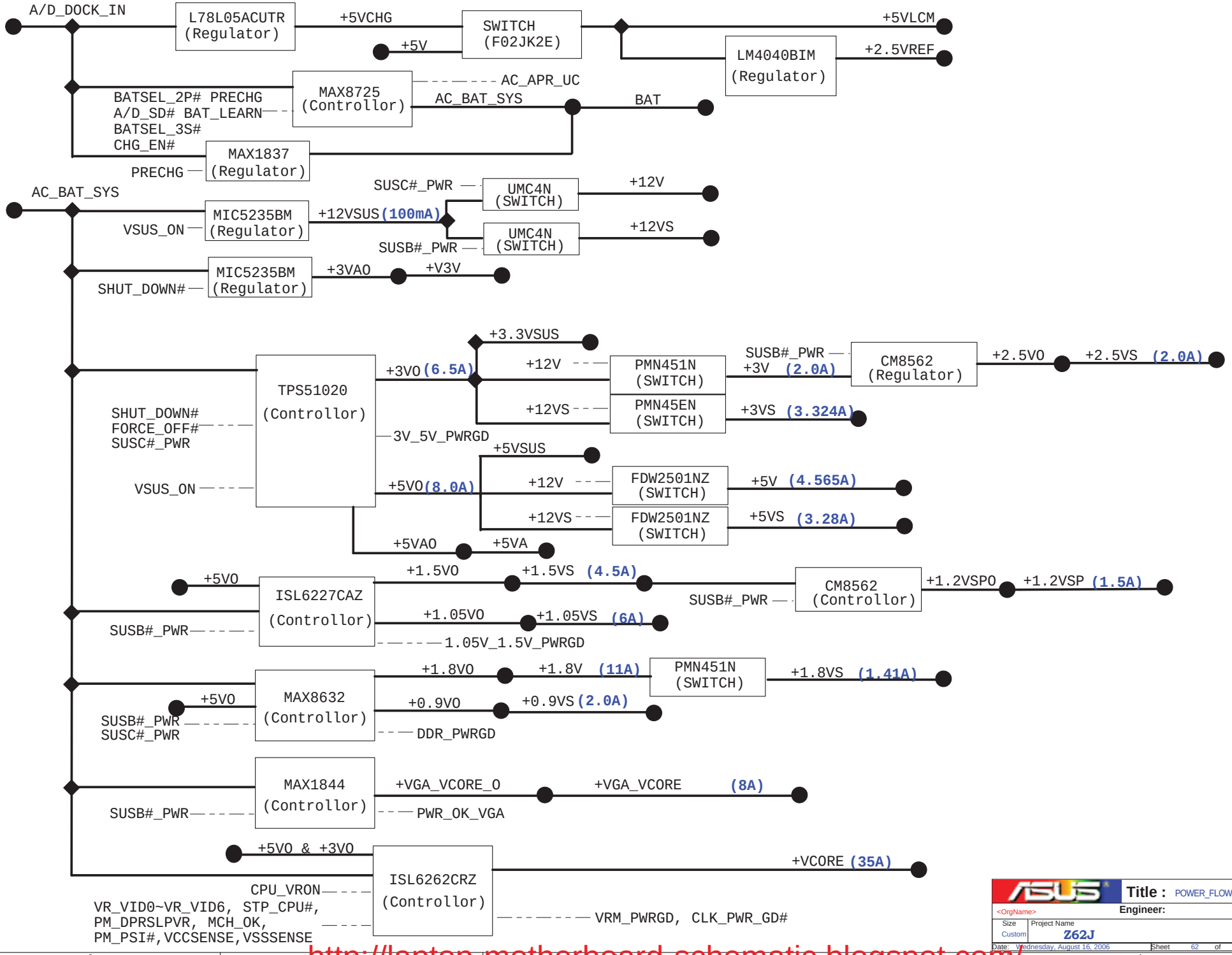
SUSB#_PWR POWER







Title : POWER_LOAD SWITCH		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 61 of 69	



AC_BAT_SYS → AC_BAT_SYS 12,50,51,52,53,54,55,57

+3VA → +3VA 4,12,20,22,28,38,54,56,59

+5VA → +5VA 51,54,56,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,61

+3VSUS → +3VSUS 18,19,20,24,28,32,35,36,37,38,51,60

+5VSUS → +5VSUS 20,36,51,60

+3V → +3V 18,19,24,26,29,30,31,32,35,40,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 4,34,35,61

+12VS → +12VS 12,13,22,35,37,56,61

+5V → +5V 12,13,16,22,30,31,34,35,36,37,40,59,61

+5VS → +5VS 4,13,19,20,21,22,27,28,35,36,37,46,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,35,44,46,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,16,35,53,61

+1.8VS → +1.8VS 35,44,47,48,49,61

+0.9VS → +0.9VS 16,35,47,53

BAT → BAT 28,57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 57,59,60

+2.5VREF → +2.5VREF 54,56,57,59,60

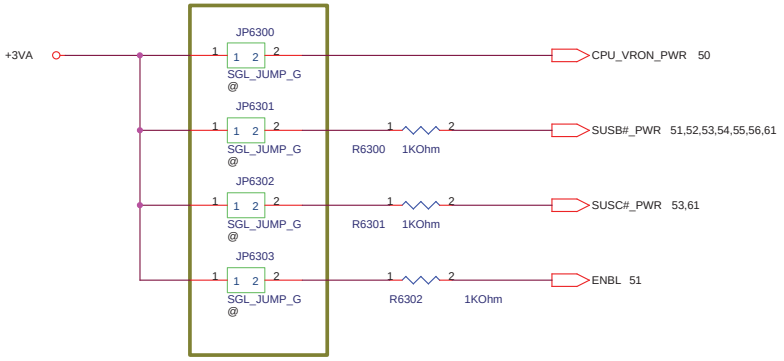
+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 39,57

+VGA_VCORE → +VGA_VCORE 42,55

+1.2VSP → +1.2VSP 35,42,47,56

FOR POWER TEST



ER_V1

Title : POWER_SIGNAL

<OrgName> Engineer:

Size	Project Name	Rev
Custom	Z62J	1.1

Date: Wednesday, August 16, 2006 Sheet 63 of 69

R1.0

Item	Before	After	Reason	Owner	Date

R1.1

Item	Before	After	Reason	Owner	Date

R2.0

Item	Before	After	Reason	Owner	Date

ASUS

Title : POWER_HISTORY

<OrgName> Engineer:

Size	Project Name	Rev
Custom	Z62J	2.0

Date: Wednesday, August 16, 2006 Sheet 64 of 69

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (TV)	AD18	0	H,G

Host	SM-Bus Device	SM-Bus Address	Device
ICH7-M	Clock Generator	1101001x (D2)	ICS954310
ICH7-M	SO-DIMM 0	1010000x (A0)	DDR SOCKET1
ICH7-M	SO-DIMM 1	1010001x (A2)	DDR SOCKET2
ICH7-M	MINI_CARD		Wireless_LAN

ICH7-M GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 0	INPUT	PM_BMBUSY#				+3VS
GPIO 1		PCI_REQ#5				+3VS
GPIO 2		PCI_INTE#				+3VS
GPIO 3		PCI_INTF#				+3VS
GPIO 4		PCI_INTG#				+3VS
GPIO 5		PCI_INTH#				+3VS
GPIO 6						+3VS
GPIO 7	INPUT	RF_OFF_SW#	**LOW**			+3VS
GPIO 8	INPUT	EXTSMI#	LOW			+3VSUS
GPIO 9	INPUT	SATA_DET#0	**LOW**			+3VSUS
GPIO 10						+3VSUS
GPIO 11	INPUT	SMBALERT#				+3VSUS
GPIO 12	INPUT	KB_SCI#	**LOW**			+3VSUS
GPIO 13	INPUT	SIO_SMI#	LOW			+3VSUS
GPIO 14	OUTPUT	802_LED_EN#	LOW	HIGH	Driven	+3VSUS
GPIO 15	OUTPUT	CB_SD#	**LOW**	HIGH	LOW	+3VSUS
GPIO 16		DPRSLPVR				+3VS
GPIO 17		GNT#5	PULL-DOWN:Boot BIOS destination select			+3VS
GPIO 18	OUTPUT	STP_PCI#				+3VS
GPIO 19	OUTPUT	PWRLED_1HZ	1 Hz	1 Hz	Off	+3VS
GPIO 20	OUTPUT	STP_CPU#				+3VS
GPIO 21		SATA0GP				+3VS
GPIO 22		REQ4#				+3VS
GPIO 23		LDRQ1#				+3VS
GPIO 24						+3VSUS
GPIO 25	OUTPUT	BT_LED_EN#	**LOW**	HIGH	Driven	+3VSUS
GPIO 26	INPUT	PCB_ID2	Default : 0			+3VSUS
GPIO 27	INPUT	PCB_ID1	Default : 0			+3VSUS
GPIO 28	INPUT	PCB_ID0	Default : 0			+3VSUS
GPIO 29		USB_OC5#				+3VSUS
GPIO 30		USB_OC6#				+3VSUS
GPIO 31		USB_OC7#				+3VSUS
GPIO 32	IN/OUTPUT	PM_CLKRUN#				+3VS
GPIO 33		AZ_DOCK_EN#				+3VSUS
GPIO 34		AZ_DOCK_RST#				+3VS
GPIO 35		SATACLKREQ#				+3VS
GPIO 36		SATA2GP				+3VS
GPIO 37						+3VS
GPIO 38	OUTPUT	BT_ON#	**LOW**	LOW	Off	+3VS
GPIO 39	OUTPUT	WLAN_ON#	**LOW**	LOW	Off	+3VS
GPIO 48		GNT#4	PULL-DOWN:Boot BIOS destination select			+3VS
GPIO 49	OUTPUT	H_PWRGD				+Vccp

ASUSTeK COMPUTER INC

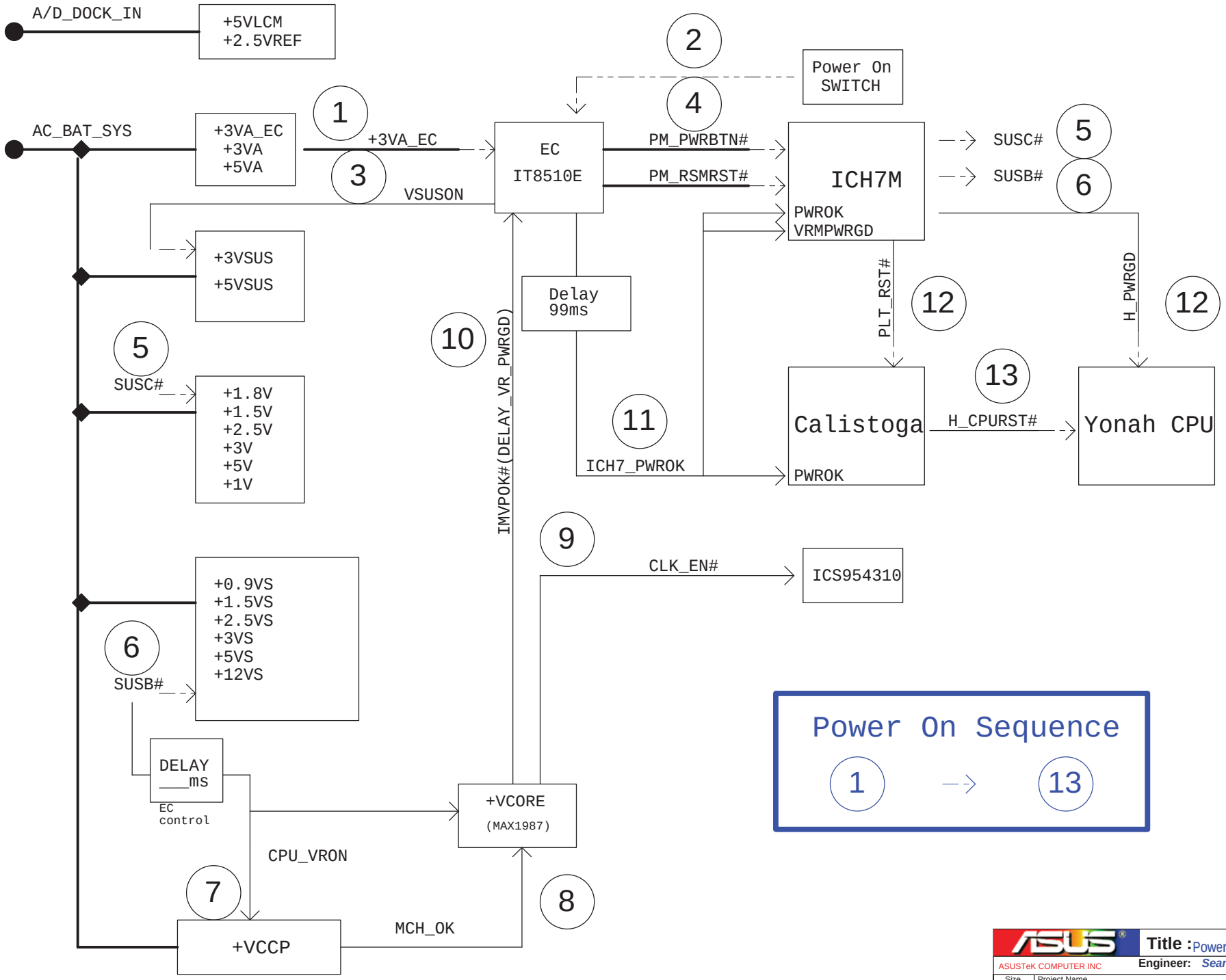
Title : System Resource

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 65 of 69

ASUSTek Computer INC. NB1	Title : History	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 66 of 69	



ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006		Sheet 67 of 69	

REVISION LIST

R1.0 2005/10/06

R1.1 2005/10/18

No 1:P39, EMI spring footprint modified

No 2:P32, Connect V_DAC bias to GLAN terminator RC: for PortBar bias issue

No 3:P43, unmount R4308 and mount R4302

No 4:P48, R4801 should change P/N to 30.1 Ohm

No 5:P12, connect the pin 30 of CON25 to +3VS

No 6:P12, mount L107 & delete L64 path; P46: add T4604

No 7:P27, ODD pin 53,54 NC

No 8:P28, delete GPA1 CHG_FULL_LED# - Bug 8

No 9:P36, Delete Q3600,R3600,R1255, Change LED5 to single color to remove charge full LED function. Connect power to +5VCHG avoid faulty GPIO control.

No10:P36, Re-assign Launch board connector pin define for correct function button

No11:P35, Re-assign Launch board pin define for correct function button

No12:P28, Add EXPLORER# instant key due to SPEC change

No13:P17, mount R206

No14:P31, delete SD_WP inverter(Q7000,R7083) - Bug 3, Bug4

No15:P23, Pre-Amp unmount - Bug 9

No16:P26, Change R2603,R2606 to 33 ohm 0603 part to avoid overshoot/undershoot

No17:P14,15, Change M_ODT[0..3]# to make correct rank ODT function

No18:P26, Delete R1059,R1060,R1061,Q141,Q142,C939,C940,L93 for BT part reduce

No19:P49, VRAM from 2 to 4

No20:P22, Change J2 connector by ID/ME's request

No21:P28, Change Con11 connector by Intel Request and redefine key matrix.

No22: Change U1's footprint to match Green Part rules. change U4,U6 part number for B0 QS samples.

No23: P24, TPM circuits modified.

No24: P7, Add R703 to support C4E Fast exist latency

No25: P39, Add R4000,R4001 unmount part to reserve pull low

No26:Green parts, JP4,7,5100,5101,5102,5400

No27: P28,38, Change R1047,R1269,R4620 to 100K ohm to reduce power consumption

No28: P28, change X8 to ROHS compliant parts.

No29: P4, P46, delete R35 & R4619; unmount Q5,Q4600; add R7091,R7092 because of no leakage current

No30: P5, P29, (1)mount C401 and change to 10pF (2) change R72 to 39ohm, (3)R77,R79,R83 change to 47Ohm. for fine clock, (4)R81 to 27Ohm

No31: P22, Change the HP mute circuits to behind decoupling capacitors for dispelling POP noise.

No32: P37, mount C1095,C1096,C1097 for EMI solution of PortBar3

No33: P46, unmount VGA thermal sensor circuits.

No34: P43, Memory strap modified

No35: P46, R4617 is changed from 300 ohm to 270 ohm to meet the 27FIX level.

No36: P27, Con10 symbol changed and pin 53,54 NC for NPTH

No37: P22, change CN1 to C2201~C2204

No38: P39, U7104~7107 change

No39: P12, P25, unmount R1201,R1202,C350,C351

No40: P39, J6 footprint changed

No41: P19, PCB_ID definition.

No42: P17, X3 capacitors change to 15 pF for accurate timing.

No43: P3, unmount CE1,CE4

No44: P22, change L31~L34 P/N

R1.2 2005/11/29

No45:P37, R818 pin1 connect to +3VSUS to solve S4 WOL fail issue

No46:P13, U80 pin16 connect to +5VSUS to solve S4 WOL fail issue

No47:P38,Delete Q135, R1051, R1054, D82, D84, C934 for reduce component

No48:P28,35,36, Delete EXPLORER# key and add back P4G instant key for PM's request

No49:P19, R156 pin1 change to +3V to meet Check list

No50:P23, mount Mic Pre-Amp for micphone volume & change C2305 to 1uF for cutoff freq. fine tune.

No51:P48, R4801 change to 40.2 Ohm for GDDR2 setting

No52: change U4 to 02G010009205, U6 to 02G010007741 for new P/N

No53: P22, add R2201,R2202 to reserve gain modification.

No54:P2,28, Add Q200 to support THRO_CPU function on to PROCHOT#.

No55:P36 : R3700 and LED5 change to connect +5VSUS to solve Battery low blinking indication no function issue.

No56:P7, Set R108 to unmount component
P28, Set D2800 to unmount component because EC do not support Watchdog

No57: P39, add U7108 for EMI spring requirement

No58: P46, add back thermal sensor

No59: P5, clock gen version changes to ICS954310CGLFT

No60: P47, add VGA termination for high speed.

No61: P12, change C756 to 0.1uF to meet LCD power sequence

No62: change all 11G232110316320 MLCC 0.01UF/10V (0402)X7R 10% to 11G232110311320 MLCC 0.01UF/16V (0402) X7R 10%

No63: P21,23, change Pre-Amp circuits because of ADI's suggest.

No64: P28, add 0 ohm at KB for EMI suggestion.

No65: P49, change VRAM from -28 to -25

No66: P32,33,37, modify LAN circuits for PortBar failure issue.

No67: P39, EMI spring footprint changed for indicating direction.

No68: P39, all screw holes except CPU bracket change to Npth.

No69: P39, R4000,R4001 mount for LIBP

No70: P21, SPDIF add a 4.7K ohm to GND

R2.0 2006/01/02

No71: P37, reserving a direct path instead of the PR/MB Lan switch.

No72: P39, changing DC Jack part and circuits for Power team's request

No73: P12, changing R813 to 47Kohm and adding R1200 for white display solution

No74: P37, updating L65 symbol and modifying all ports' properties, including power curcuits

No75: P47, add two 0.1uF and unmount all the terminations

No76: P37, unmount switch ralative 3 components, and mount all 2R4P 0ohm

No77: P48, change R4801 to 30.1 OHM back from nVidia(No51)

No78: P28, use capacitors instead of KBC beads for cost down and EMI

No79: P20, 38, add test point T2000, T3800

No80: P31, add MS Duo protect circuits

No81: P22, Change R265,R266 to 30Kohm to meet Speaker's SPEC

No82: P35, change R7000~R7003 to 220 ohm to meet 5ma current

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1
MINIPCI(TV)	PCI_REQ#0

IDSEL

MINIPCI	PCI_AD19
CB&1394	PCI_AD17
10/100	PCI_AD16
MINIPCI(TV)	PCI_AD18

ASUSTeK COMPUTER INC

Title : Revision List

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

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REVISION LIST (2)

No83: P28, add and reserve R2804, R2805
No84: P46, use GPIO9 to moniter temperture.
No85: P37, delete reseverd analog switch circuits.
No86: delete 0 Ohm:
R195,703,102,2000,462,469,2400,2403,458,2800,347,349,387,391,7084,7085,4202,3903,359,404,466,507,1259,3200,160,206

R2.1 2006/02/23
No87: P42, add 0 ohm back : R4202,R466,R507,R404.
No88: P46, unmount thermal sensor circuits
No89: P33, mount C893, C894 for PR EMI concern
No90: P27, unmount R345, mount R346 for setting CDROM master
No91: P39, H41 change footprint to PHI=6.9 for factory issue.
No92: P35, add +1.2VSP and +1.8VS discharge circuits
No93: P34, add R3400 and unmount R435 and Q47
No94: P2, unmount CE54, CE8, CE19, CE15 and change VCORE 22uF to 10uF
No95: P29,P42, U25 U4200 footpoint change to nb_
No96: P22, R1267, R1268 are from 0 ohm to 22 ohm to fix audio volume bar issue.
No97: P5, unmount R507
No98: P31, change L42 footprint for lower height
No99: P35,P39, H4001,4004,4008,4012,7000,7001 change to NPTH
No100: P12, change C756 to 0.22uF to reduce CMO power off garbage.

post R2.1 2006/05/03
No101: P9, add 150uF on CE8
No102: P36, TP switch change P/N

Z62JM R2.2
change some circuits for Vista and PortBar LAN

Z62JM R2.3 2006/08/09
ER NO1: P22 mute circuits inverted for vista default driver
ER NO2: P22 solve external pop noise, +12VS delay, add C2205 and D2200, and change R270 to 1M ohm
ER NO3: P34, solve external USB power leakage
ER NO4: P9, change 150uF to 330uF for CMOS data lost
ER NO5: P22 solve internal pop noise, R271=470K, C2206=2.2uF

ASUSTeK COMPUTER INC	Title : Revision List (2)	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 69 of 69	